analog dialogue

A forum for the exchange of circuits, systems, and software for real-world signal processing

COMPLETE MONOLITHIC VOLTAGE-OUTPUT μP-COMPATIBLE 12-Bit DAC (page 7)

Single-Port 16 × 16 Multiplier-Accumulator Saves Hardware and Real Estate (page 3)

Flash Converters Work Better with Track/Holds (page 10)

Complete Contents on Page 3

Volume 18, Number 2, 1984

ANALOG DEVICES

Editor's Notes

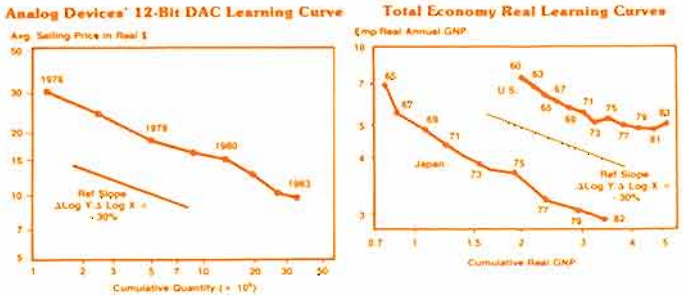
PRODUCTIVITY & LEARNING

"There is no limit to learning, there is only what we settle for."

With these words, President and Chairman Ray Stata concluded his 1984 address to Analog Devices shareholders.[1] The gist of his message was that: the organization learning curve is a universal means of measuring learning performance (and thus productivity) among organizations of all sizes, from product lines to national economies; its slope is a measure of competitiveness, and increasing the slope by improving organizational learning is not only possible but should be a major objective of progressive organizations. The objective of Analog Devices is to evolve from its present flatness to 7.5% to 12.5% annual growth in real productivity for 25% growth in real sales.

The product-cost learning curve, developed through empirical observations by the Boston Consulting Group, has shown that real value-added costs—for a wide range of products—decline by 20% to 30% every time *cumulative* product volume doubles. Plotted on a log-log scale, this function approximates a straight line with a slope of about −0.2 to −0.3. The left- hand figure shows the learning curve for 12-bit d/a converters at ADI, with selling price (real dollars) used as a proxy for value added.

At ADI, we have extended this concept to embrace organizational learning. The "output" of the organization is the value added to the costs of things bought, transformed, and sold to customers. The "cost" of the organization is the human effort to produce the value-added, viz., "cost in employee-years per $million of value-added." Since employment grows, negative slope of the "organizational learning curve" means that value-added grows even faster. The counterpart of the decline in the cost curve is an increase in its reciprocal, *productivity*, i.e., "$million of value added per employee-year"; a falling learning curve implies *increasing productivity*, and we are more concerned with the rate of increase than the actual datum at any time. As the organization learns, value-added increases with cumulative value-added experience.



Applying the concept to total economies, the right-hand figure compares organizational learning curves for Japan and the U.S.A., measured by (employment)/(real annual GNP) vs. cumulative real GNP – with GNP as a proxy for value added. It is evident that the learning curve for Japan's economy is both steeper and more consistent than that of the U.S., which currently shows a "bottoming" tendency (productivity "topping-out.")

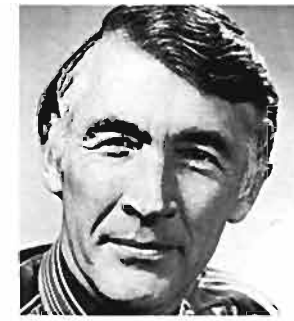
[1]Use the reply card to request a copy of the complete message, containing many charts and equations (by ADI Vice President A. Graham Sterling) and presenting economic information in a light that is both unusual and eye-opening.

Improving the slope of the learning curve, using a measure of value added meaningful to the organization, is a worthwhile objective that will improve the ability of a growth-oriented organization to compete and produce real benefits for its employees. ADI believes that this can be done and is committed to it for the future.

The elements of ADI's program to increase organizational learning are: Vision (top management must not impede employee self-motivation); Participation (in the ideal case, each worker should be his or her own manager); Alignment (every employee should understand the purpose of his or her job in terms of the final results to be achieved); Quality improvement (the causes of defects and process variations should be understood and eliminated—"do it right the first time"); Long tenure (knowledge is carried in people's heads, turnover is detrimental to organizational learning); Assimilation and training (education and training programs for employees must be effective); and Investments in capital and technology (ability of workers to produce must be enhanced by the availability of up-to-date tools). ▶

Dan Sheingold

THE AUTHORS



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(Continued on page 26)

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ADSP-1110: SINGLE-PORT 16 X 16 MULTIPLIER-ACCUMULATOR

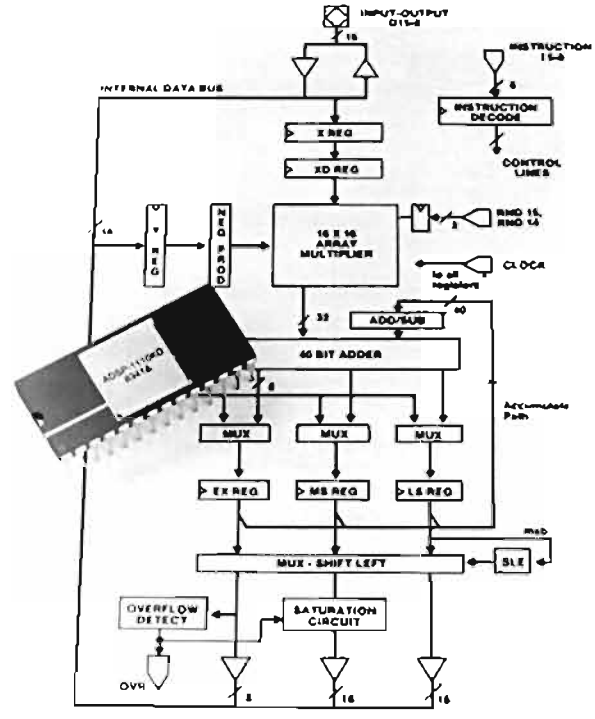
Save Hardware Costs and Real Estate in Digital Signal Processing

28-Pin DIP with Unusual Arithmetic Capabilities for Compact DSP Designs

by John Oxaal

Although prices of integrated circuits for digital signal processing (particularly digital multipliers) have been coming down, high price and large circuit-board footprint have tended to restrict their use to applications where performance is required without regard to the costs. The introduction of CMOS for DSP components by Analog Devices and others has brought a welcome reduction of dissipation, but there are still problems. A standard three-port 16 × 16-bit multiplier-accumulator (MAC), for example, costs well over one hundred dollars; and the 64-pin package required for connecting to its three 16-bit data ports (two inputs and one output), plus power and controls, consumes considerable real estate. In addition, conventional 16-bit MACs suffer from restricted arithmetic capability, making them cumbersome to use.

The new ADSP-1110* eliminates these problems of three-port MACs. All data is handled via a single 16-bit bus, in response to a sophisticated 6-bit instruction set. The single-port structure allows it to fit into a 28-pin DIP, which makes DSP substantially more cost-effective with little sacrifice of throughput. The smaller package costs less to manufacture and reduces board-space requirements by nearly a factor of four, compared to 64-pin packages. Its cost is less than half that of conventional 16-bit MACs, $75 in 100s.



ABOUT MULTIPLIER/ACCUMULATORS

Digital multiplier/accumulators (MACs) play a fundamental role in what has come to be known as digital signal processing. The core DSP tasks—filtering, spectral estimation via fast Fourier transforms (FFT), correlation, and matrix multiplication are characterized by chains of multiplications, the results of which are accumulated. A good example is the well-known FIR (finite impulse-response, or non-recursive) filter equation (Figure 1, see also page 8):

$$y(n) = \sum_{m=0}^{N-1} h(m) \cdot x(n-m) \qquad (1)$$

Each output point, y(n), is obtained by accumulating the results of N multiplications between coefficients, h(m), and data, x(n − m). Three-port MACs have been employed for years to perform these functions. But, as mentioned, three-port MACs are expensive, make inefficient use of board space and require external logic chips to make up for their arithmetic deficiencies.

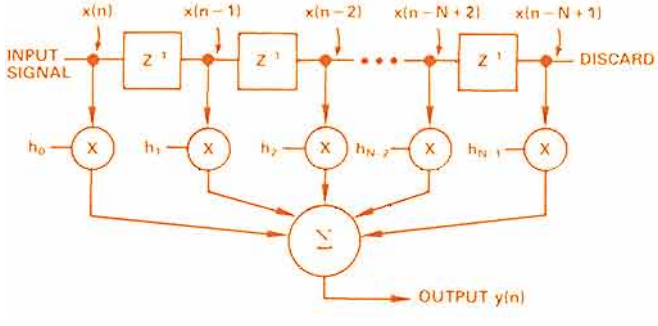


Figure 1. Finite impulse-response filter architecture.

*Use the reply card for technical data.

IN THIS ISSUE

Volume 18, Number 2, 1984 – 28 Pages

Editor's Notes, Authors (more authors on page 26) . . . 2
Single-Port Multiplier-Accumulator Saves Hardware and Real Estate (ADSP-1110) . . . 3
The Compleat General-Purpose 12-Bit D/A Converter (AD667) . . . 7
Speed Up FIR Filters . . . 8
Flash Converters Work Better with Track/Holds . . . 10
First 12-Bit, 1-MHz Hybrid A/D Converter with Track/Hold (HAS-1201) . 15
Generate Precision Square and Triangular Waves with AD630 Balanced Modulator/Demodulator . . . 16
Flexible Monolithic Instrumentation Amplifier (AD625) . . . 19
Thermocouple-Based Setpoint Controllers (AD596 and AD597) . . . 20
Autoranging Microprocessor-Based RTD/Thermistor Meters (AD2060/61) . 21
New Hybrid Resolver-to-Digital Converter Family (1S20/40/60/61) . . . 22
Low-Cost 12-Bit Analog Interface Boards for VMEbus (RTI-600) . . . 23
New-Product Briefs:
16-Bit Hybrid A/D Converter (AD ADC71/72) . . . 24
8 × 8 Monolithic CMOS Multiplier with Unsigned Format (ADSP-1081) . 24
Low-Cost Precision FET Op Amp (AD611) . . . 24
Double-Buffered 14-Bit CMOS Multiplying DAC (AD7534) . . . 25
Analog Devices "Eye" Intelligent Vision System (IVS-100) . . . 25
Power Oscillator for Resolvers (OSC1758) . . . 25
Worth Reading—New Publications from Analog Devices, ADI in Trade Press . . . 26
Porpourri . . . 27
Advertisement . . . 28

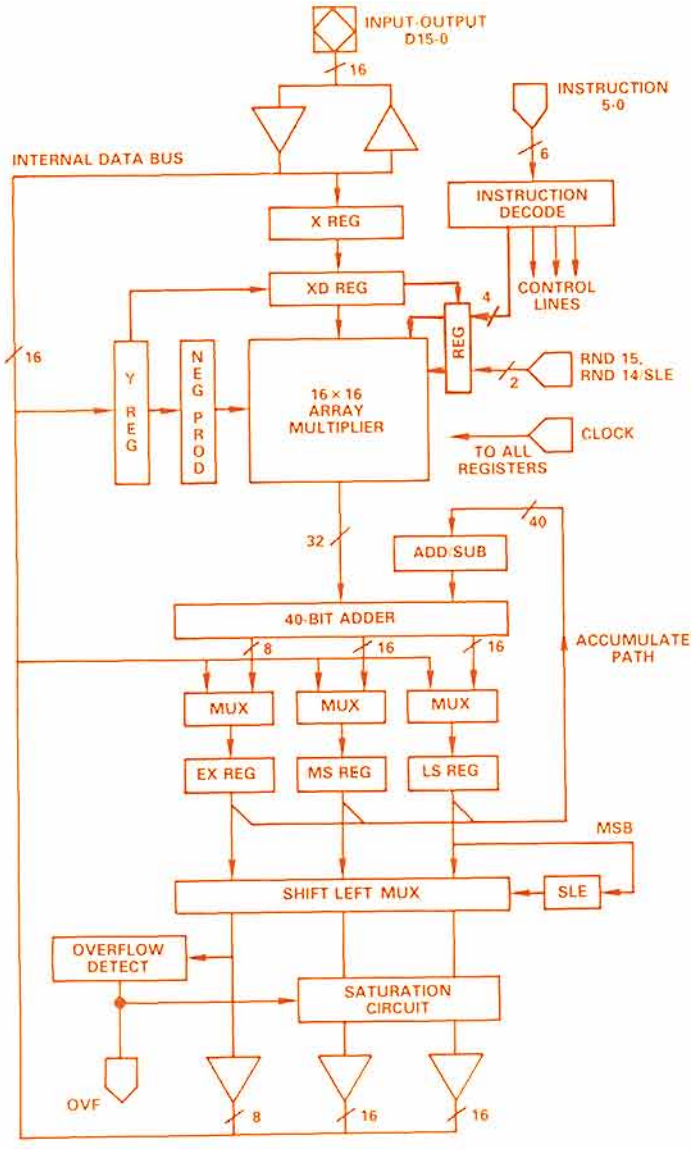


Figure 2. Block diagram of the ADSP-1110.

Figure 2 shows the architecture of the ADSP-1110. The single 16-bit I/O port handles the 16-bit X and Y inputs, 16-bit more-significant product (MSP), 16-bit less-significant product (LSP), and the 8-bit extension—which allows up to 256 full-scale products to be summed without danger of losing information.

The time required to perform the multiply-accumulate operation is 200 ns (over the entire −55°C to +125°C ambient temperature range), and 100 nanoseconds is required for I/O. In two 100-nanosecond cycles, the device can load new X and Y inputs, while concurrently performing a multiply/accumulate on previous input data. For DSP calculations, which typically require only infrequent outputs, this scheme results in an average time of only slightly more than 200 ns per operation. Furthermore, as will be discussed, many on-board "hooks" save both external hardware and I/O cycles.

To understand why throughput is not sacrificed in DSP applications, consider the case of a 90-tap FIR filter. As illustrated in equation 1, each output sample would require 90 separate multiply/accumulate operations. A typical three-port CMOS MAC, such as the ADSP-1010, features a multiply time of 200ns over temperature, so a 90-tap FIR filter calculation requires (90)·(200ns), or 18μs per output sample. The ADSP-1110 single-port MAC, in the same application, requires 100ns to load the first x value, (90)·(200ns) for the multiply-accumulates (multiplication occurs simultaneously with the y input), and 100ns to output the 16 most-significant-product bits. The total time to output the result is thus 18.2μs, only 1% slower than a three-port device.

Other interesting benchmark operations that will be discussed in the applications section are: 1.1μs per IIR biquad (infinite impulse-response—or recursive—filter section); 10ms per complete 1024-point *complex* FFT; and, 4μs for multiplying a 4 × 4 matrix by a 4 × 1 matrix.

While offering all the arithmetic functions of the three-port device, the single-port MAC boasts several unique (among MACs) features that simplify numerical calculations. These include:

- *A 40-bit accumulator* with overflow detection and overflow flag. This feature is especially useful for many-tap FIR filters.
- *The option of conditional (on the overflow flag) saturation on output*, i.e., permitting the output to saturate instead of rolling over on a carry. Saturation on overflow minimizes the deleterious effects of wraparound (e.g., when trying to go from +FS to +FS + 1, the output actually goes from +FS to −FS in twos-complement arithmetic). Among the problems associated with it, wraparound can cause full-scale oscillations in an IIR filter.
- *Shift left on output* allows the redundant sign bit to be removed and a digit of precision to be gained in twos-complement multiply-accumulate operations.
- *Independent controls for rounding in either the 14th or 15th product bit* allow rounding consistent with either a shifted or unshifted output. The combination of shift left and rounding on the 14th bit allows one to obtain a properly rounded 15-bit plus sign twos-complement output.
- The ADSP-1110 provides *negative product logic*, which allows the designer to obtain ± product ± accumulator. This feature is quite useful to obtain multiplication by +1, i.e., (−1)·(−product), which can't be done in twos complement with standard MACs.
- A single-bit shift-left-extend register increases the precision obtainable in double precision operations.
- The ability to transfer the MS (more-significant) register to the LS (less significant) register and the EX (extension) register to the MS register is useful for table look-up operations and rotate and merge functions.

While not all these features will be useful for every application, they will in general (as shown in the following applications section) reduce the external logic elements and attendant power and board-space costs associated with the standard three-port designs.

APPLICATIONS

The following examples describe applications of the single-port MAC in traditional DSP benchmark calculations. They will show that the ADSP-1110 provides, on a single chip in a 28-pin package, the characteristics needed in an arithmetic processor—without significant performance penalties. We will first describe IIR filters, then FFTs and matrix multiplications.

IIR Filter

Recall that, in the equation for a biquad section of an IIR filter, for the 0th (i.e., present) point,

$$y(0) = a_0x(0) + a_1x(-1) + a_2x(-2) - b_1y(-1) - b_2y(-2) \quad (2)$$

where y(0) and x(0) are the present output and input, $y(-1)$ and $x(-1)$ are the last values of y and x, and $y(-2)$ and $x(-2)$ are the next previous values, as shown in the block diagram of Figure 3.

While most of the coefficients can be scaled to be equal to or less than unity, b_1 often ranges in value from 1 to 2. The most convenient way to represent the coefficients and data is in fractional twos-complement notation. Since this numbering system only ranges from -1 to $+0.999...$, all the coefficients and data for the IIR filter have to be divided by 2, in order to handle the larger values of b_1 when using a conventional MAC. Then, at the output, external shifters are needed to shift the result up 1 bit (or re-multiply by 2).

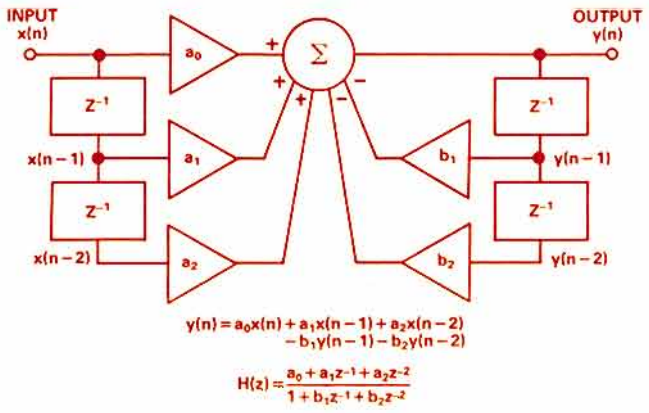


Figure 3. Infinite impulse-response filter biquad section.

With the single-port MAC, however, a coefficient in the $+2$ to -2 range is available by means of a mixed-mode multiplication (unavailable with standard MACs) which has an output with twice the magnitude of a twos-complement multiply. A multiply-and-add—or a multiply-and-subtract—provides the correct choice of sign as the product enters the accumulator, an option unavailable with other MACs; the result is multiplication by a constant from -2 to $+1.99...$

A problem with IIR filters (as with any system that has feedback) is that, because of "wraparound" in twos-complement arithmetic, certain combinations of data and coefficients (even though the filter is theoretically stable) can induce full scale oscillations in the filter. The hard limiting provided by the ADSP-1110's saturation arithmetic prevents oscillations due to overflow.

Simplifies FFT Butterflies

Single-port MACs are of great use in implementing "butterflies"—the key arithmetic operation in computing fast Fourier transforms. The FFT is a powerful algorithm used to greatly reduce the number of complex multiplications in performing a digital Fourier transform (i.e., from N^2 to $(N/2)\log_2(N)$—for example, from more than one million ($1{,}024^2$) to 5,120, for a 1024-point transform—a factor-of-200 reduction.

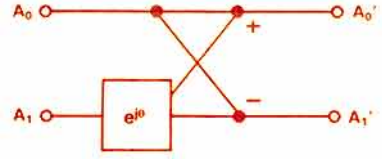


Figure 4. Fast-Fourier-transform "butterfly".

The characteristic flow diagram of a basic FFT computational unit, or "butterfly," is shown in Figure 4, for a decimation-in-time computation. In the general case, all variables and coefficients are complex, leading to a typical pair of equations of the form,

$$\begin{aligned} A_0' &= A_0 + A_1\epsilon^{j\theta} \\ A_1' &= A_0 - A_1\epsilon^{j\theta} \end{aligned} \quad (3)$$

the complex number A_1, multiplied by a rotation, $R = e^{j\theta}$, is added to the complex number, A_0, to produce A_0', and subtracted from A_0, to produce A_1'. By properly sequencing the butterflies, you obtain an FFT. A 1024 point FFT, for example, contains about 5000 butterflies. The rotation, R, can be written

$$\begin{aligned} e^{j\theta} &= \cos\theta + j\sin\theta \\ &= C + jS \end{aligned} \quad (4)$$

If A_0 and A_1 are complex numbers,

$$\begin{aligned} A_0 &= X_0 + jY_0 \\ A_1 &= X_1 + jY_1 \end{aligned} \quad (5)$$

then,

$$\begin{aligned} A_1 e^{j\theta} &= [X_1 + jY_1][C + jS] \\ &= [X_1C - Y_1S] + j[X_1S + Y_1C] \end{aligned} \quad (6)$$

The outputs, A_0' and A_1', are also complex, i.e.,

$$\begin{aligned} A_0' &= X_0' + jY_0' \\ A_1' &= X_1' + jY_1' \end{aligned} \quad (7)$$

From (3) and (6), their real and imaginary parts are computed as follows:

$$\begin{aligned} X_0' &= X_0 + (X_1C - Y_1S) \\ Y_0' &= Y_0 + (X_1S + Y_1C) \\ X_1' &= X_0 - (X_1C - Y_1S) \\ Y_1' &= Y_0 - (X_1S + Y_1C) \end{aligned} \quad (8)$$

To complete the butterfly, a number of multiplications, additions and subtractions must be performed.

When using a single-port MAC to perform butterflies, begin by placing X_0 into the accumulator; simply multiply by positive full scale, or 0111111111111111. Compute X_0'

$$X_0' = KX_0 + X_1C - Y_1S \quad (9)$$

where K = 0111111111111111. Then, noting that X_0' is equal to $2X_0 - X_1'$,

$$X_1' = 2KX_0 - X_0' \quad (10)$$

where X_0' is the accumulator's contents, and $2KX_0$ results from a mixed-mode multiplication of 2K and X_0. This operation represents a multiply-and-subtraction which (unlike other available MACs) the single-port MAC readily handles. The imaginary terms, Y_0' and Y_1' are computed in the same way.

Table 1 provides the details of the process for computing an FFT butterfly with a single-port MAC. For each point, ten cycles are required to compute the real component, plus ten more cycles for the imaginary part. At 100ns per cycle, the total time required is 2.0 microseconds. A 1,024-point FFT, requiring about 5000 butterflies, takes 10 milliseconds.

An FFT calculation contains a series of multiply/accumulates and multiply/subtracts. This presents a challenge in rounding the result, because rounded inputs from earlier cycles become inputs for later cycles. The rounding on cycles 4, 6, 14, and 16 ensures that the outputs (on lines 7, 10, 17 and 20) are rounded correctly.

Lines 4 and 14 round on bit 14 to prepare for a left-shift during

Table 1. Computing Sequence for Single-Port MAC Butterfly

Cycle #	Operations	Acc Reg Contents
18′	Load K	
19′	Load X_0 & Mult	Previous $KY_0 - X_1S + Y_1C$ + RND14
20′	Output MS Reg left-shifted (previous Y_1′)	
1	Load C	
2	Load X_1 & MAC	KX_0
3	Load S	
4	Load y_1 & Neg Mult & ACC + RND14	$K_0X_0 + X_1C$
5	Load 2K	
6	Load X_0 & Mult & Neg ACC + RND15	$K_0X + (X_1C - Y_1S)$ + RND14
7	Output MS Reg (X1′) left-shifted	
8	Load K	
9	Load Y_0 & Mult	$K_0X - (X_1C - Y_1S)$ + RND14
10	Output MS Reg (X_0′)	
11	Load S	
12	Load X_1 & MAC	KY_0
13	Load C	
14	Load Y_1 & MAC + RND14	$KY_0 + X_1S$
15	Load 2K	
16	Load Y_0 & Mult & Neg Acc + RND15	$KY_0 + (X_1S + Y_1C)$ + RND14
17	Output MS Reg (Y_1′) left-shifted	
18	Load K	
19	Load X_0(new) & Mult	$KY_0 - (X_1S + Y_1C)$ + RND14
20	Output MS Reg (Y_0′) left-shifted	

output. However, lines 6 and 16 round on bit 15. This is necessary because, in performing the multiply and subtract on these lines, the original round on lines 4 and 14 becomes inverted—it becomes a subtraction of one, rather than an addition of one. For compensation, 2 must be added to the 14th bit: 1 to compensate for the previous round, and then 1 to round the current result. This can be easily accomplished in one step by adding a 1 to bit 15 rather than to bit 14. Thus, the result in MS continues to maintain the correct rounded result after further accumulations.

To prevent overflow during FFT calculations, the overflow flag can be used. The overflow flag is set when a bit in the EX register differs from the sign bit in the MS register. The combination of the overflow flag and the MAC's saturation arithmetic ameliorates the disastrous consequences of overflow in the FFT calculation.

Use Single-Port MAC To Upgrade Graphics Systems

Matrix multiplications are used in numerous applications; examples include modern motion controllers and graphics systems. In a bit-mapped graphics system, matrix multiplications are used to implement a variety of image manipulations such as translation, rotation, and zoom. The ADSP-1110 Single-Port MAC makes an ideal accelerator for speeding up the performance of matrix multiplications for a microprocessor-based graphics system.

Here's an example: Points on an object are rotated abut the Z-coordinate axis to new positions by setting the new x,y coordinates – X′,Y′ – to: $X' = x\cos\theta + y\sin\theta$ and $Y' = -x\sin\theta + y\cos\theta$. For the homogenous three-dimensional transformation

$$P(x,y,z) \longrightarrow P(X',Y',Z')$$

where P(x,y,z) is the original point, whose coordinates are x,y, and z, and P(X′,Y′,Z′) is the transformed point, the following matrix is computed.

$$[X,Y,Z,1]\begin{bmatrix} \cos\theta & -\sin\theta & 0 & 0 \\ \sin\theta & \cos\theta & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix}$$

The transformed point is equal to the row, [x, y, z, 1], multiplied by the transformation matrix, and:

$$X',Y',Z' = [x\cos\theta + y\sin\theta,\ -x\sin\theta + y\cos\theta,\ z]$$

In general, a translation matrix, a scaling matrix, and a rotation matrix are concatenated to yield an overall transformation matrix, (for which some—or most—of the zero elements above would become non-zero). In any case, the ADSP-1110 can multiply a 4 × 4 matrix and 4 × 1 vector (requiring 16 MACs) in less than 4 µs.

Conclusion

We have shown here that the single-port MAC has the hooks necessary to perform the varied tasks of the number-crunching section of a DSP system with reasonable performance. Filtering, FFT's, matrices for graphics, and other operations are all done at a fast clip on a single chip. The savings in parts count, parts cost, board space and power dissipation—with acceptable speed for many cases—make the ADSP-1110 an ideal choice as an arithmetic processor in compact systems.

Interpreting Digital Multiplication Results

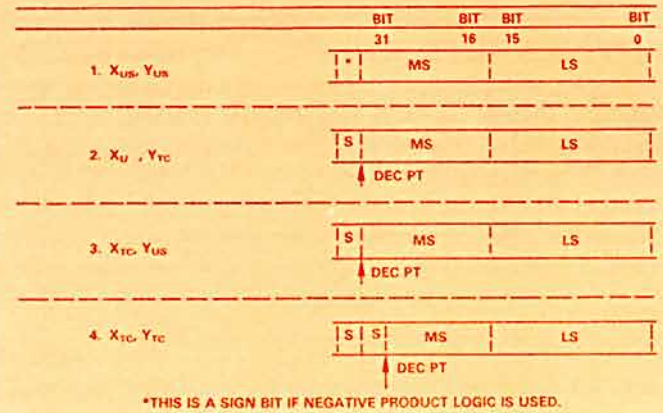
When performing digital multiplications with devices such as the single-port MAC, the results you get will depend on whether the inputs, X and Y, are unsigned or signed (twos-complement) numbers.

There are four possible input combinations:

	X	Y
1.	Unsigned	Unsigned
2.	Unsigned	Twos complement
3.	Twos complement	Unsigned
4.	Twos complement	Twos complement

The figure below illustrates the results of the multiplication for each of the above four cases. Note how the two most-significant bits of the MS register differ, depending on the case. The results of cases 2 and 3 have only a single sign bit. As a result of twos-complement arithmetic, on the other hand, case 4 has two sign bits, and the "decimal" point is shifted down by one position. However, this is not a problem; because the single-port MAC has left-shift capability at its output, the result of case 4 can be reformatted to have only 1 sign bit and 30 magnitude bits.

The left-shift capability can also serve to upscale both signed and mixed-mode numbers.



THE COMPLEAT GENERAL-PURPOSE 12-BIT D/A CONVERTER

Monolithic AD667 Has Voltage Output, Linearity to ½-LSB over Temperature
Internal Reference, 3-μs max Settling, Double-Buffered μP-Compatible Input

by Doug Grant and Steve Lewis

The evolution of high-linearity 12-bit digital-to-analog converters in integrated-circuit form has constituted a long, arduous climb. Significant landmarks on the bipolar-technology route were the AD550 quad switches (1970), the AD562 two-chip current-output DAC (1974), the AD565 internal-reference monolithic DAC (1978), the AD567 double-buffered current-output DAC (1982), and —now—the summit has been reached, in the form of the AD667*, a completely self-contained monolithic device which does not require a single support component to perform its function.

UNIVERSAL MONOLITHIC DAC

The AD667 (Figure 1) complete, voltage-output d/a converter has its own on-chip high-stability buried-Zener voltage reference, double-buffered digital latches that are compatible with 4-, 8-, 12-, and 16-bit data buses, and a fast output amplifier with five user-configurable output ranges. It will operate at voltages from ±11.4 to 16.5 V dc and typically dissipates less than 300 mW when operated from ±12-volt supplies.

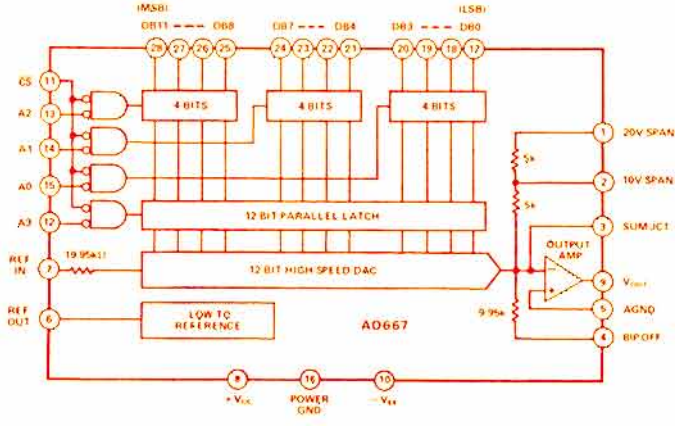


Figure 1. AD667 block diagram.

Its completeness, versatility, speed, accuracy, choice of packaging options, and low price make it a first choice for any application calling for a fixed-reference "no-problem" bus-compatible 12-bit d/a converter.

Versatility: The AD667's positive-true digital data inputs are compatible with both TTL and 5-volt CMOS logic. Divided into 3 4-bit quads, they accept input data in a sequence of 4-bit nybbles from 4-bit buses, 8 + 4 or 4 + 8-bit bytes (left- or right-justified – see Figure 2) from 8-bit buses, and 12 bits in parallel from 12- or 16-bit buses. The inputs are double-buffered—this means that the converter may be updated when all 12 bits have been loaded, avoiding spurious analog output values. The control signals may be arranged for automatic updating when the full 12-bit word has been loaded. In addition, a group of DACs may be updated simultaneously or in any desired sequence after having been loaded asynchronously by any of the above schemes. Since the latches are level-triggered, they may be hard-wired in a transparent mode.

*Use the reply card for technical data.

The AD667's 10-volt (±1%) reference, which is externally jumpered to the device input, with typically 1 mA to spare, may also serve other devices or as a system reference. The AD667's output voltage may be pin-programmed for bipolar outputs of ±2.5 V, ±5 V, or ±10 V, and unipolar outputs of +5 V or +10 V, at up to 5 milliamperes. The AD667's connection scheme permits a current booster to be connected inside the output op-amp's loop for high-current applications (e.g., line driving).

Speed: The use of precision high-speed bipolar current-steering switches and an on-chip high-speed output amplifier results in a 10 V/μs slew rate and settling time of 3 μs maximum to within ±½ LSB for a 10-volt output change; for 1-bit changes, typical settling time is 1 μs. The digital latch responds to strobe pulses as short as 100 nanoseconds, allowing the device to be used with fast microprocessors.

Accuracy: All versions of the AD667 have guaranteed monotonic behavior over the specified temperature range. The AD667K and AD667B guarantee maximum linearity error of ±¼ LSB at +25°C and maximum differential and integral linearity errors of ±½ LSB over temperature. Initial gain error is 0.2% of full scale (max) and offset is 2 LSB (max), while maximum temperature coefficients are ±15 ppm of full-scale range per °C for gain, ±3 ppm/°C for offset, and ±10 ppm/°C for bipolar offset.

Packaging Options: The AD667 is offered in five grades, J/K for 0°C to +70°C, A/B for −25°C to +85°C, and S for −55°C to +125°C. J/K versions are provided in 28-pin proven plastic DIPs, and the other grades are available in a choice of hermetically sealed ceramic DIPs or 28-terminal ceramic leadless chip-carriers (LCCs). Prices, the lowest in the industry, start at $9.90 in 1000s ($11.95 in 100s) for the AD667JN.

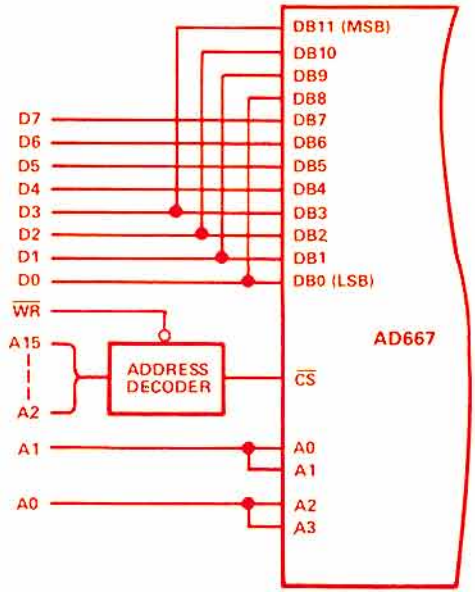


Figure 2. Connections for right-justified 8-bit bus interface.

SPEEDING UP FIR FILTERS (MAKING THE FIR FLY)

When Coefficients Exist in Symmetric or Antisymmetric Pairs Symmetry Can Be Used to Speed up Computation by Factors of 2

by Per E. Pedersen and Bill Windsor

Editor's Note: In *Analog Dialogue* 17-2 (1983), we published an article[1] discussing a simplified design method for digital finite impulse-response (FIR, or non-recursive) filters. In response to the article, and to our invitation to readers to join in the *Dialogue*, Per E. Pedersen, of Hellerup, Denmark, sent us a note suggesting a way of speeding up implementation of the design discussed in the article. In these pages, the earlier article is recapitulated and Mr. Pedersen's valuable suggestion is explained.

FIR FILTER-DESIGN BASICS

Both analog and digital filters pass signals in a specified frequency range and attenuate signals outside that range. But digital filters operate on discrete data—that is, sampled data in digital form, obtained either from stored data of any kind retrieved in the form of a time series or from conversions of electrical signals to digital by an a/d converter.

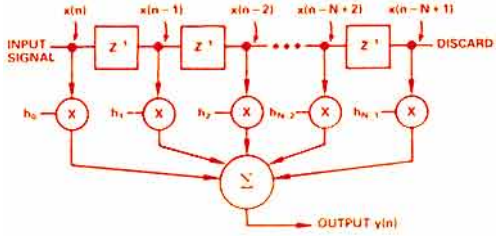


Figure 1. Block diagram of direct-form FIR filter (N-tap filter).

The digital filter can operate on the data in the time domain by performing numerical calculations to implement the filter's equation. As Figure 1 shows, the output of an FIR filter is the sum of a series of multiplications of filter coefficients, h(m), and the corresponding sampled input-data points, x(n − m). If the filter has N coefficients, or taps, N multiplications will be required on the N most-recent signal samples. The coefficients, which constitute the indicial time response, or the discrete Fourier transform of the desired frequency response, are usually generated by a computer program[2]. The equation for an FIR filter output at the *n*th sample point (instant of discrete time) is:

$$y(n) = h(0)\cdot x(n) + h(1)\cdot x(n-1) + \ldots + h(N-1)\cdot x(n-N+1)$$

$$y(n) = \sum_{m=0}^{N-1} h(m)\cdot x(n-m) \qquad (1)$$

For example, if the filter has 27 taps and we are computing the value of y(100), the first term of the sum will be h(0)·x(100) and the last term will be h(26)·x(74). This series of multiplications and additions performs the convolution of the input signal with the filter coefficients. The output values are available for storage, further processing, or conversion to analog with a d/a converter.

[1] "Digital FIR Filters Without Tears," by Bill Windsor and Paul Toldalagi, *Analog Dialogue* 17-2 (1983), pp. 12-19.

[2] A FORTRAN program to generate FIR filter coefficients is available free of charge. Write to Analog Devices, DSP Marketing, One Technology Way, Norwood MA 02062. Request the "Remez Exchange Application Note."

In the direct form of Figure 1, there are N multipliers, and each data point can be computed as rapidly as data can be shifted, the multiplications performed in parallel, and the sum taken in real time. Generally, such rapid computation (and high expense) is not warranted; a single multiplier will still compute each point several orders of magnitude faster than multiplication in software.

In one implementation (Figure 2), the input signal is sampled using the a/d converter, and the discrete data are stored in the RAM. The coefficients are stored in PROM. The counter addresses values of coefficients and corresponding input data, and feeds these values to the multiplier. The pointers step sequentially through memory to access the coefficients and data. The multiplier computes the products, which update the sum in the accumulator. After all multiplications have been performed, the output value for the point then computed is read from the accumulator.

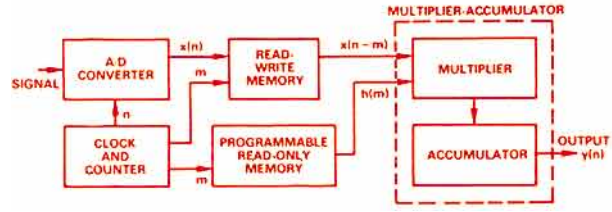


Figure 2. FIR filter employing a hardware multiplier.

Linear Phase and Symmetric Coefficients

Besides being simpler in concept and easier to design than digital filters in other forms, FIR filters can be made to have a linear phase response, resulting in a constant time delay for all frequency components. Besides being useful in many applications requiring preservation of waveshapes, linear phase response is accompanied by symmetric coefficients. *Symmetric* coefficients have mirror symmetry about the ordinate at the midpoint of the range of N coefficients; corresponding *antisymmetric* coefficients have odd-value symmetry (equal magnitudes but opposite polarity).

The set of coefficients h(n) is determined from the desired frequency characteristic of the filter; for example, for an ideal low-pass filter (Figure 3), with rectangular magnitude transfer function, H(f), and linear phase, the inverse Fourier transform, h(n), will be of the form, sin x/x, comprising real coefficients having mirror symmetry about the central term. Although the sin x/x function

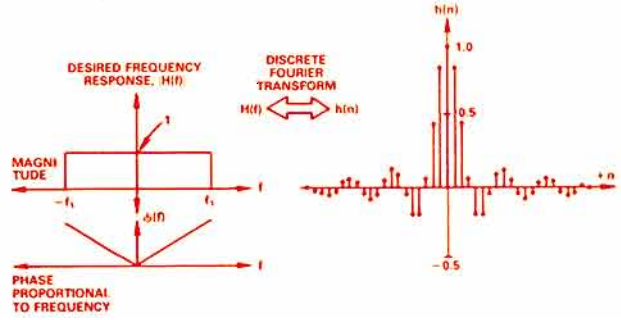


Figure 3. Filter coefficients, h(n), derived from the frequency response, H(f).

has an infinite number of terms, the filter as designed will have a finite number of terms, N, arbitrarily truncated via a *windowing* function, but still symmetrical.

Although h is time-shifted, to establish its leftmost element as h(0), at m = 0, such a time shift is simply equivalent to a linearly increasing phase shift in the frequency domain, leading to a fixed delay in the response.

Design Improvement

Symmetrical coefficients lead to a substantial improvement in design of a digital filter, because

$$h(0) = h(N-1), \quad h(1) = h(N-2), \quad \text{etc.} \tag{4}$$

Since addition is distributive, we can take pairs of terms of (1), starting with the outermost terms, and compute them by adding the x's in pairs and multiplying them by the common factor—thus saving one multiplication per pair of terms. This is done by inserting an adder ahead of the multiplier/accumulator (MAC), shifting about half of the computational burden to the adder.

$$y(n) = h(0)[x(n) + x(n-N+1)] + h(1)[x(n-1) + x(n-N+2)] + \ldots + \text{final term} \tag{5}$$

For an even number of coefficients, the final term is the (N/2)th term, equal to (since the first term is h(0)):

$$h(N/2-1)\{x(n-N/2+1) + x(n-N/2)\} \tag{6}$$

The block diagram is shown in Figure 4a. If there are an odd number of coefficients, the final term is the ((N+1)/2)th term, equal to

$$h((N-1)/2))[x(n-(N-1)/2)] \tag{7}$$

The corresponding FIR filter block diagram is shown in Figure 4b.

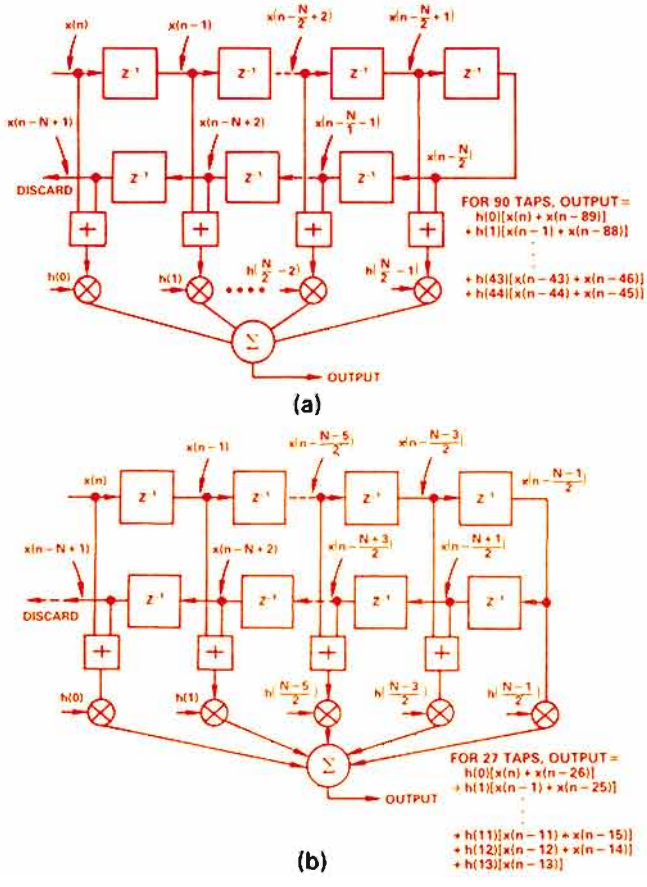


Figure 4. FIR filter block diagrams for symmetric coefficients. (a) Even number of taps. (b) Odd number of taps.

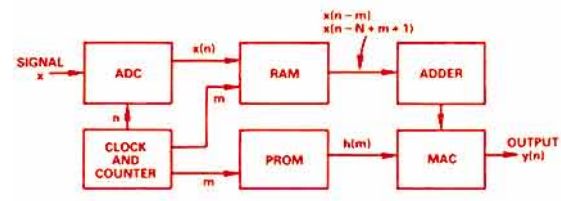


Figure 5. Hardware architecture of the filter.

If the filter coefficients are anti-symmetric, the pairs of magnitudes of x are subtracted instead of being added. A hardware configuration to implement this add-then-multiply scheme is shown in Figure 5. Figure 6 outlines the pointer scheme, similar to Figure 9 of Reference 1, to implement the add-then-multiply FIR filter.

The speed increase for the FIR calculation is significant. In a benchmark test, using a PDP11/03 system and software multiplication, computation time was reduced from 28.6 to 13.6 milliseconds per computed value of the output, y(n), for a 27-tap FIR-filter subroutine—and to 11.9 ms with direct addressing.

With hardware multipliers, the high speed they make available is also approximately doubled. An N-multiplication FIR design, using a 16 × 16-bit ADSP-1010 multiplier/accumulator (165ns per multiply/accumulate) yields an execution time—for a 32-tap FIR—of 5.28 microseconds. The add-then-multiply approach, using an ADSP-1010 for the MAC and four Fairchild 74F283's for the adder (36ns per 16-bit add), yields an execution time for a 32-tap FIR of 2.68μs. Part of the speed improvement in the add-then-multiply approach results because the clocked input registers of the MAC act as a pipeline register between the adder and the MAC stages of the hardware. Thus, at the cost of minimal additional hardware, the add-then-multiply approach attains an almost twofold improvement in speed over the direct-form implementation of the FIR.

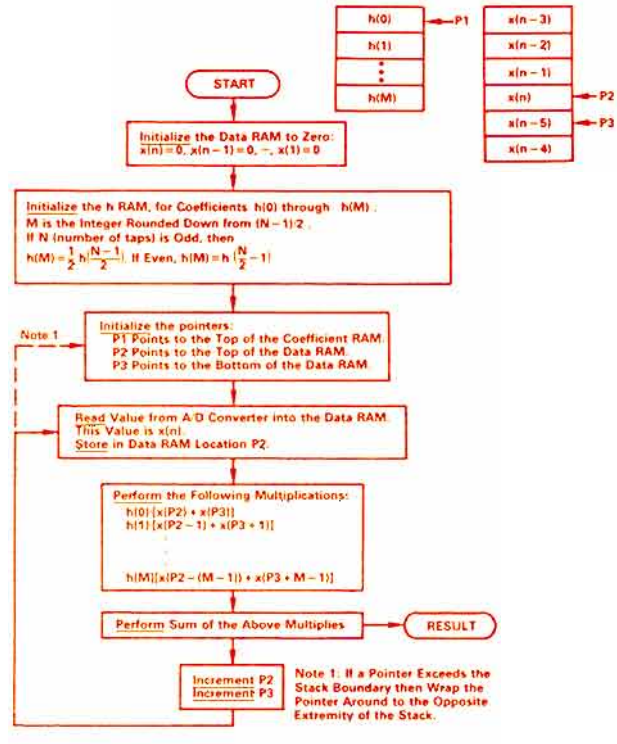


Figure 6. Pointer scheme to implement add-then-multiply FIR filter.

FLASH CONVERTERS WORK BETTER WITH TRACK/HOLDS

There Is Less Distortion of High-Frequency Signals
Conversion Is Performed with Better Linearity and Few (If Any) Missed Codes

by Jerry Neal and Jim Surber

High-speed analog-to-digital "flash" converters (ADCs) are coming into widespread use. Although they provide the promise of "instantaneous" conversion, and their latching systems would appear to make track-holds unnecessary, it has long been our opinion that they would perform closer to their full dynamic potential when used with fast track-holds. Until now, users have had few options because of the rarity of really fast T/H's, but with the recent introduction of the HTS-0010* (*Analog Dialogue* 18-1, 1984), it is now feasible to enjoy the benefits of track/hold with flash converters.

In this article, we report on the results of a Computer Labs study of the possibility of improving flash-ADC performance by employing a fast track-hold amplifier. Not to leave you in suspense, the magnitude of the improvement, at both fast and slow encode rates, is remarkable. Even low-resolution (6-bit) flash-converter circuits can benefit.

Read on if you wish to learn: why flash ADC circuits benefit from track/hold signal conditioning; about two test methods for verifying performance improvement; how to select and implement track-and-hold amplifiers for use with flash converters.

WHY FLASH CONVERTERS NEED TRACK/HOLDS

Traditionally, flash converters have been used without a track/hold amplifier, because the internal latches of the converter perform a track/hold function. However, there are distinct advantages in using a T/H for signal conditioning ahead of the converter, because the analog comparison may not yet be valid at the time the decisions are latched.

Figure 1 shows a typical converter subsystem. The function of a track/hold amplifier at the input of a sampled-data system is to follow all changes in the analog input as they occur ("track" mode) and periodically capture an instantaneous sample of that input ("hold" mode) for additional signal processing. The change from *track* to *hold* is accomplished with an encode command by the user; the trailing edge of that command returns the unit to the track condition to await the next encode command.

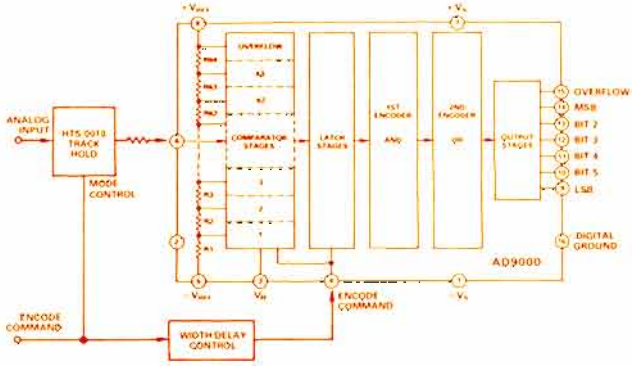


Figure 1. Typical flash ADC-track/hold subsystem.

*Use the reply card for technical data.

Track and *hold* alternate during each strobe period; the *hold* interval is established by the time allotted for conversion, and the *track* interval is the remaining portion of the strobe period. The sampling rate (1/strobe period) is limited at the high end by the time required for the track/hold to acquire the analog signal and settle to a sufficient degree of accuracy.

The ability of the track/hold amplifier to freeze a fast-changing analog signal, i.e., to transform it into a set of successive dc voltages, is the characteristic which permits the T/H to enhance the performance of flash converters.

Flash ADC's use $2^{(n-1)}$ comparator cells to perform the parallel flash conversion. Certain inherent characteristics of these cells tend to degrade the performance of the flash converter as the analog input frequency and/or the encode rate are increased.

As Figure 2 shows, each comparator has a differential input—with the analog input signal on one side and a reference voltage on the other. The reference voltage, or switching threshold, at a different level for each comparator, is established by the voltage divisions of the reference-resistor ladder.

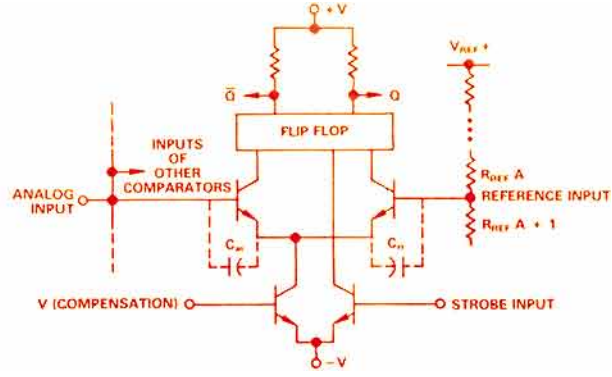


Figure 2. Typical flash-converter comparator cell.

All flash converters have inherent capacitance characteristics that affect their ability to operate on high-frequency analog signals. There are sets of problems that are specific to each of the inputs.

The analog input capacitance (C_{ai}) of each comparator is determined primarily by the base-emitter junction capacitance of the transistor on the analog-input side. The value of this capacitance is affected by junction bias; forward-bias capacitance is higher than reverse-bias capacitance. Since the inputs of all comparators are in parallel, the total capacitance at the flash converter's analog input is the sum of the individual comparators' base capacitances.

Unfortunately, the total capacitance is essentially random, because it depends on the amplitude of the analog signal: the signal amplitude and the on-off state of each individual comparator dictate its base-emitter voltage, hence its contribution to the total capacitance. The total capacitance can vary from 30 to 120 pF.

Since the comparator can be driven by an analog buffer, this is not a serious problem. However, the buffer doesn't solve capacitance problems associated with the reference input.

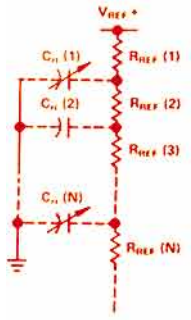


Figure 3. Equivalent circuit of the reference-resistor ladder.

Since the comparator has a differential input, the reference input is similarly subject to capacitance variations introduced by its base-emitter capacitance, C_{ri}. But the problems they raise are not as easily dealt with; see Figure 3.

The charging path for each individual C_{ri} is through the reference ladder. This charging path constitutes an R-C time constant at the reference input; and the time required to charge the capacitances through the resistors tends to cause the reference voltages to lag fast changes in the current flowing through the reference ladder, dynamically distorting the voltage division of the reference ladder.

This capacitive reactance effect depends on the differential input voltage to the comparator, the speed at which it varies (frequency), and the comparator's position within the ladder. When signals having high slew rates are applied, the a-c integral-linearity error of the comparator array will increase because of the reactance variations among the many comparators.

In addition, errors also occur due to noise introduced by parasitic coupling from the strobe circuit to the reference ladder via C_{ri}. Although the strobe is equally coupled to both sides, the lower source impedance at the analog side tends to reduce its amplitude, resulting in an imbalance between the comparator inputs.

One of the most effective ways to equalize the differential input impedances of the comparators is to use an external resistor in series with the analog input of the converter, as Figure 1 shows, to produce better common-mode rejection of unwanted noise voltages and improve the integral linearity of the comparator array. The resistance value should be about one-fourth of the total resistance of the reference ladder (i.e., the parallel resistance of the upper and lower halves of the ladder resistance).

Another potential source of dynamic conversion error in flash ADC designs is the variation of effective sample delays. Individual comparators within an array can be visualized as having variable delay lines in series with their latch inputs. The magnitude of delay for each comparator is determined by comparator inconsistencies, chip layout, and the strobe frequency.

For low-frequency analog inputs, these sample-delay variations among adjacent comparators are not a significant problem. But as the input frequency is increased, latch-time disparities among comparators can result in missing codes and excessive differential nonlinearities. The errors differ with slew-rate magnitude and direction.

Many manufacturers and users of flash converters loosely define this variable-slew-vs.-latch error as "aperture-time uncertainty" or "jitter." That terminology can be misleading if a "jitter" specification does not include the total sample delay variations among the comparators. The misconception becomes readily apparent when the relationship of the maximum bandwidth (slew rate) of a flash converter to its specified aperture jitter is considered.

For a ½-LSB error tolerance in the design of a flash converter, the maximum rate of change is (τ_a = max aperture jitter)

$$dV/dt_{max} = \tfrac{1}{2}\text{LSB voltage}/\tau_a \quad (1)$$

An undistorted sine wave's rate of change is

$$dV/dt = 2\pi f V_p \cos(2\pi f t) \quad (2)$$

where V_p is the peak amplitude of the sine wave. The maximum rate of change, occurring at the zero crossing, is

$$dV/dt_{max} = 2\pi f_{max} V_p \quad (3)$$

Substituting (3) in (1), and recognizing that $\frac{1}{2}\,\text{LSB} = 2^{-(n+1)} \cdot 2V_p$, where n is the converter resolution,

$$f_{max} = 2^{-(n+1)}/\pi\tau_a \quad (4)$$

Thus, for an 8-bit converter with a specified aperture jitter of 30 picoseconds, one would expect a maximum large-signal bandwidth of 20.7 MHz. It is interesting to note that, for a commercially available 8-bit device with this specified aperture jitter, the maximum bandwidth is specified at only 7 MHz.

This disparity between the calculated bandwidth—using the aperture-jitter specification—and the bandwidth the vendor is willing to guarantee indicates that "aperture jitter" is not the crucial factor in the sample-delay variation of a flash converter. Performance evaluations of several models of flash converters have led to the practical conclusion that it would be more realistic to expect sample-delay variations as large as 200 to 300 picoseconds rather than to calculate them based on published aperture-jitter specifications.

They also suggest that there is room for improvement, if we can replace the sample-delay variations of a flash converter by the much faster performance characteristics of a sample-hold. For example, the Analog Devices HTS-0010 track/hold amplifier is specified to have an aperture uncertainty of 5 ps, in contrast to the 50-or-more picosecond sample-delay variation of a typical flash converter.

Since the track/hold ahead of the flash converter freezes the input signal, it maintains a constant input while the comparators are latching, and it can also be timed to allow the comparator input capacitances to charge and settle before the conversion takes place.

It is important to remember that a track/hold amplifier used ahead of a flash converter has no effect on the conversion time; it simply allows the converter to digitize higher-frequency (faster slew rate) analog signals. The total time required for conversion, taking into account the delays of both the track/hold amplifier and the flash converter, can be calculated and compensated for by the system timing.

TESTING COMPARATIVE PERFORMANCE

AC linearity tests concretely demonstrated the improvement of performance gained by teaming a flash converter with a track/hold amplifier. The parameters tested were harmonic distortion and differential linearity. Both test series demonstrated excellent performance improvement for converters of all resolutions—at all encoding rates.

A real-time spectrum analyzer provided a basis for judging the improvement in harmonic distortion. An input waveform was con-

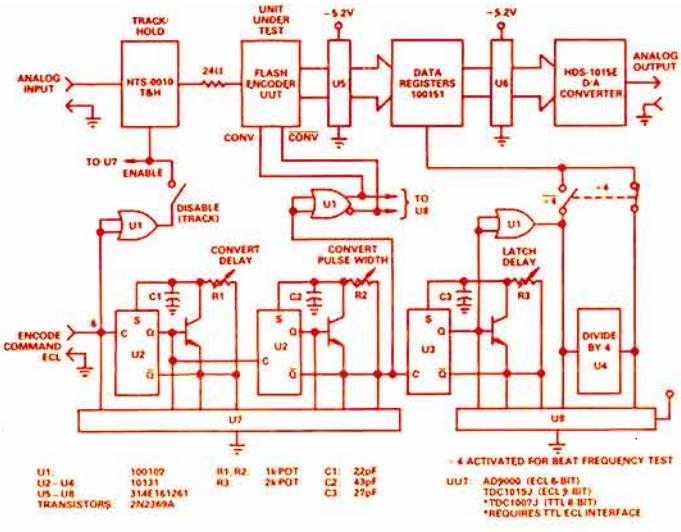


Figure 4. Test fixture for converting and reconstructing analog waveforms at high speed.

verted to digital, then reconstructed, using the test fixture of Figure 4. The measurement instrumentation consisted of a Hewlett-Packard model 8553B RF-section/8552B IF-section spectrum analyzer, for displaying the frequency spectrum of interest.

The sampling bandwidth of the spectrum analyzer was limited to 3 kHz, to maximize the dynamic range of the analyzer and make the test results easier to interpret. If the sample bandwidth is too high, the quantizing noise level can mask the harmonics and make it more difficult to determine their precise amplitudes.

The *encode* command, buffered through U1—wired as shown—generates the track/hold command; its duty cycle determines the *hold* time. Strobes for the flash-encoder and the data-registers are generated by one-shot multivibrators; they are used to control the timing and width of the flash converter's strobe—and the timing of output data being applied to the register.

Elements U5 and U8 are resistor strips, which supply Thévenin equivalent terminations for the high-speed ECL signals being used. They were selected because they are easy to use, and their characteristics are compatible with good high-speed-design practice. At the output of the test fixture, a high-performance, 10-bit ECL-compatible d/a converter minimizes the amount of DAC-contributed error at the frequencies of interest.

Harmonic-Distortion Test. In the harmonic-distortion test, the flash ADC encodes a full-scale sine-wave input at various selected

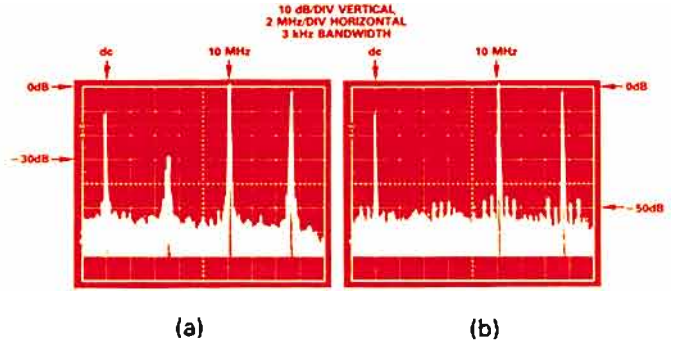


Figure 5. 6-bit flash converter output-spectrum display, 25-MHz encode rate, 10-MHz analog input. (a) Track/hold inactive. (b) Track/hold active

frequencies. The d/a converter in the test fixture reconstructs the digital output of the ADC into an analog representation of the input. The reconstruction is then measured for harmonic content on the analog spectrum analyzer. Although the harmonics themselves are out-of-band, they produce beat frequencies that appear in-band.

In the first test, a 6-bit flash converter (AD9000) was encoded at 25 MHz, with a 10-MHz sine-wave input. With a word rate of 25 MHz, the frequency band of interest is from dc to 12.5 MHz, for Nyquist conversion. It is desirable for all frequencies in this band to be well below the amplitude of the input signal. As Figure 5a shows,* with the T/H inactive (i.e., in the track mode), or even completely bypassed, the highest component in this band is 29 dB below full scale.

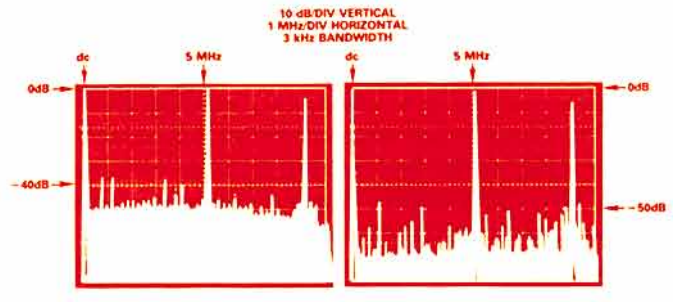


Figure 6. 9-bit flash converter output-spectrum display, 14-MHz encode rate, 5-MHz analog input. (a) Track/hold inactive. (b) Track/hold active.

When the T/H is activated (i.e., switched between *track* and *hold*, with a 25 ns strobe, the highest harmonic component in the band measures 45 dB below full scale (Figure 5b). The AD9000 used in this test was selected for excellent linearity (within ±¼ LSB), which resulted in low harmonic content. The test demonstrates than an input track/hold amplifier is beneficial, even for a 6-bit flash operating at relatively slow word rates.

Another harmonic distortion test was performed with a 9-bit flash converter (TDC1019J), encoded at 14 MHz with a 5-MHz full-scale sine-wave analog input. For this test, the frequency band of interest is from dc to 7 MHz. With the T/H inactive (Figure 6a), the in-band harmonics measure 39 dB below the fundamental. Figure 6b shows that activating the track/hold amplifier results in a 9-dB improvement of in-band harmonics—a significant improvement. Tests performed with an 8-bit flash (TDC1007J) indicated performance improvement commensurate with that of the 9-bit flash.

Beat-Frequency Test. This test demonstrates the converter's high-speed differential-linearity characteristics. The method used is to encode the converter's full-scale sinewave analog input at a frequency differing from the input frequency by precisely 2 kHz. Successive samples of the encode command step slowly through the

*A bit of guidance may be desirable in interpreting these spectral plots: First, note that dB scales are logarithmic; there is no "zero." Hence, all that frightening-looking stuff at the bottom of the figure is pretty far down; the highest error peaks are the only ones to be concerned about. In Figure 5a, the peak at dc is a marker to indicate the location of dc; the peak at 15 MHz represents a beat between the 10 MHz signal and the 25 MHz sampling frequency - it is out of band; and the one at 5 MHz is the result of a beat between the 15 MHz beat and the 10 MHz signal. Note that, on the logarithmic scale, each bit of resolution corresponds to 6.02 dB. However, these results are not intended to imply absolute harmonic-distortion performance of the various flashes, just comparative performance with and without T/H.

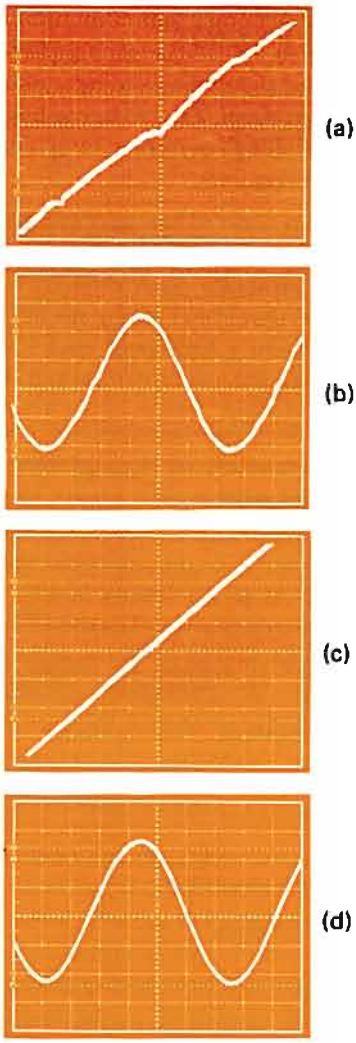


Figure 7. 8-bit converter linearity with 9.998-MHz input, 10-MHz encoding rate. (a) Major-carry linearity, T/H inactive. (b) Output waveshape, T/H inactive. (c) Major-carry linearity, T/H active. (d) Output waveshape, T/H active.

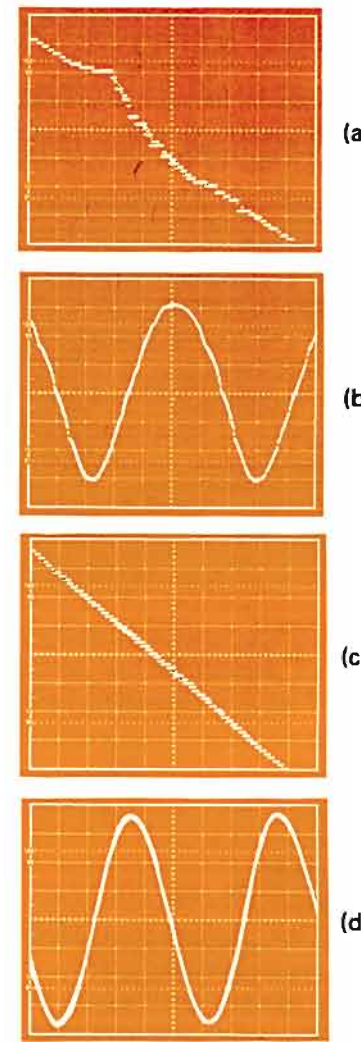


Figure 8. 8-bit converter linearity with 19.998-MHz input, 10-MHz encoding rate. (a) Major-carry linearity, T/H inactive. Note multiple missed codes. (b) Output waveshape, T/H inactive. (c) Major-carry linearity, T/H active. (d) Output waveshape, T/H active.

sinewave input at the 2 kHz beat rate, and the ADC yields an output sinewave at the beat frequency. In effect, we are purposely creating a 2-kHz alias which, nevertheless, shows the errors of the conversion, such as missing codes and differential nonlinearities which are occurring at a much higher frequency and would be much harder to capture in a high-speed reconstruction.

A modulo-4 counter is incorporated in the test setup to look at every fourth sample, an arbitrary measure to make it easier to synchronize the oscilloscope waveform. The relatively slow beat code is reconstructed with a slow, accurate d/a converter and displayed on an oscilloscope.

The first test was of an 8-bit TDC-1007J flash converter. The ADC strobe width was 20 nanoseconds, applied to the converter 15 ns after the leading edge of the *encode* command. The track/hold amplifier was activated with a 23-ns hold pulse. In all tests, the analog input was a crystal-controlled full-scale sinewave of the appropriate frequency; the encode command, crystal-controlled but asynchronous, was set at a frequency 2 kHz higher than the analog input.

Figure 7 shows the test output with an encoding rate of 10 MHz and a 9.998-MHz sine wave applied. Without the T/H, the sinewave is visibly distorted (b), and the actual linearity errors and missing codes are quite apparent (a). When the T/H is activated, the clean waveforms of (c) and (d) result. The code-spacing now seems almost perfect, with greatly improved overall linearity.

Figure 8 shows the test output for the same ADC with an encoding rate of 20 MHz and a 19.998 MHz sine-wave input. Here, the display (a) and (b) shows even greater anomalies in the flash output because of the higher slewing rate of the analog input. But again, with the T/H activated (c) and (d), the errors disappear and the integrity of the reconstructed signal is materially improved.

The above tests were repeated with a 9-bit flash converter (TDC1019J) and displayed the same kind of degradation/improvement results in high-speed differential linearity.

SELECTING AND USING A TRACK/HOLD AMPLIFIER

Careful selection of the correct track/hold amplifier and a few design precautions will help the designer ensure successful operation of a flash converter-track/hold combination. The encoding rate limitation for the units working together can be calculated:

$$f_{max} = 1/(T_A + T_S + T_h) \qquad (5)$$

where f_{max} is the maximum encoding frequency, and T_A and T_S are the acquisition and settling times to the desired resolution

(track/hold specification), and T_h is the hold-time necessary for the flash converter to set up (flash converter specification).

The large-signal bandwidth of the track/hold amplifier must also be high enough to accommodate the analog input signal without attenuation. For example, the 40-MHz analog bandwidth of the HTS-0010 is commensurate with Nyquist operation of most available flash converters.

For best performance, the track/hold amplifier and the flash converter should be mounted on a massive ground plane, as close to one another as possible. All ground pins must be connected together and to the ground plane, close to the case. Decouple the track/hold amplifier power-supply leads from ground with a 0.01-μF ceramic capacitor *and* a 10-μF electrolytic capacitor. These connections should be made right at the supply pins of each device. It is also mandatory to isolate the analog and digital inputs physically for proper high-speed performance.

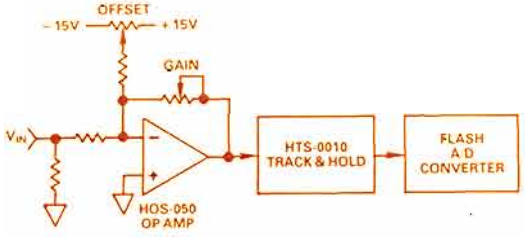


Figure 9. Input signal conditioning with HOS-050 op amp.

Some flash converters work best with a unipolar input range such as 0 to +2 V, or 0 to −2V. Since many applications use bipolar sources, some sort of signal conditioning is often necessary to scale and offset the input signal. This can be combined with buffering through the use of a high-performance op amp, such as the HOS-050*, as shown in Figure 9.

Adhere to the guidelines outlined here to obtain better initial performance and reduce the time needed for "cleaning up" the circuit layout. Applications assistance from manufacturers is readily available, and designers should make use of this help, whether they are planning to implement a high-speed track/hold amplifier, a flash converter, or some combination of these and other devices.

CONCLUSION

When maximum ac performance is required from a flash ADC, a fast track/hold amplifier at the input is a *must*. The T/H performs the signal-acquisition function and allows the flash ADC to operate in essentially a dc mode. As the test results shown here illustrate, flash converters of all resolutions benefit from an input track/hold amplifier, even at relatively low conversion frequencies.

One final *caveat*: Since all systems are unique, the engineer is strongly encouraged to evaluate the track/hold amplifier in the actual final design application. This technique is the only true guarantor of performance and guardian against surprises.

*Use the reply card for technical data.

UNDERSTANDING TRACK/HOLD AMPLIFIER TERMINOLOGY

Acquisition Time An indication of how fast the track/hold can be updated, it is the total time required for the charge on the storage capacitor (and, in most cases, the output voltage) of the track/hold amplifier to reach a specified error band about its final value, after the control input is switched from *hold* to *track*. Included are the times required for switching, slewing, and capacitor charging to within a specified tolerance.

Aperture (delay) time The mean time required for the switch in the track/hold amplifier to become fully open after the *hold* command is applied. The actual sample of the analog voltage being held is delayed by this amount; the timing of the *hold* command can be advanced to take the aperture delay time into account. This interval does not vary from one sample to the next within a given T/H; since it can be compensated for, it does not contribute to errors in the held value of a regularly sampled voltage.

Aperture Uncertainty (jitter) The sample-to-sample variation in the track/hold's aperture time. Caused by noise, phase shifts, and other unpredictable factors, it is augmented by the jitter of any time marker affecting the system aperture time. A random phenomenon, aperture jitter cannot be compensated for by timing adjustments. It can cause errors in the held value of voltage from one sample to the next. The contribution to aperture jitter is a critical specification for a T/H amplifier.

Bandwidth The maximum frequency which can be transmitted by the track/hold amplifier with less than (or equal to) 3 dB of attenuation. It is expressed in MHz for high-speed devices.

Charge Transfer See Pedestal.

Droop Rate The rate at which the held value at the output of the T/H amplifier changes during the time the unit is in the *hold* condition, as a result of leakage or bias currents flowing in either direction through the hold capacitor; its polarity depends on the sources of droop. In devices requiring external capacitors, it is often specified as a maximum current ($I = C\,dV/dt$).

Feedthrough The fraction of the ac input waveform or fast signal variations that appears in the held output value of the track/hold amplifier in the *hold* mode; it is caused by stray capacitive coupling from the input to the storage capacitor, principally across the open switch. This value is generally expressed in terms of dB below full scale.

Pedestal (also known as *charge transfer*, *offset step*, or *sample-to-hold* error) A measure of charge transferred to the hold capacitor via stray capacitance when switching to the *hold* mode. The charge causes a shift in the level of the sample voltage which is being held. Pedestal voltage is reduced by lightly coupling a version of the *hold* command signal in opposite polarity for cancellation. In devices with fixed internal capacitors, it is expressed in millivolts; otherwise in picocoulombs.

Settling time The time required for the output of the T/H amplifier to reach its final value, within some error band (usually expressed as per cent of full-scale), when the unit makes a change from *track* to *hold*.

FIRST 12-BIT, 1-MHz HYBRID A/D CONVERTER WITH TRACK-HOLD

HAS-1201 Is Complete in 46-Pin Hermetically Sealed DIP

Two-Step Flash Unit is Ready to Go, Needs only Power and Encode Commands

WHY COMBINE A TRACK/HOLD WITH AN ADC?

As the preceding article (page 10) has noted, track/hold is essential to accurate conversion at high sampling rates, even with "flash" converters, because of the converter's sample-delay variations. A good track/hold stage, with low aperture jitter, freezes the rapidly varying input signal, converting it momentarily to a "dc" signal, long enough for a fast converter to deal with it.

To demonstrate the necessity of track/hold in high-speed conversion (as well as at surprisingly low speeds), consider this: the highest sine-wave frequency, f_H, that can be digitized with predictable ½-LSB resolution, with a given aperture uncertainty, τ_a, is

$$f_H = 2^{-(n+1)}/\pi\tau_a \qquad (1)$$

For n = 12 bits and τ_a = 100 ns, f_H is about *389Hz*. In order to digitize a 389 *kHz* sine wave (about the highest frequency you'd want to digitize at a 1-MHz sampling rate) to this degree of resolution, the aperture uncertainty would have to be less than 100 ps. A track/hold can be used to achieve this; in the HAS-1201*, the aperture delay time is 30 ns, and the uncertainty is 80ps.

The strong rationale for the HAS-1201, the coming standard 1-MHz 12-bit converter, is: since the track/hold is necessary, why not have it on-board? For this to happen with specified performance, all sorts of parts-procurement, noise, timing, layout, and interconnection problems are resolved by the converter manufacturer (instead of the user). This allows the manufacturer to optimize the components as a subsystem, providing a synergism that is otherwise unavailable to the end user.

THE HAS-1201

The HAS-1201 is the first complete commercially available 12-bit, 1-MHz converter with track/hold in a hybrid package; it requires only power and an encode command. After receiving an encode command, the HAS-1201 generates the necessary internal timing commands to hold the signal, control the two-step flash conversion process, and load the data into the output three-state latches.

*Use the reply card for technical data.

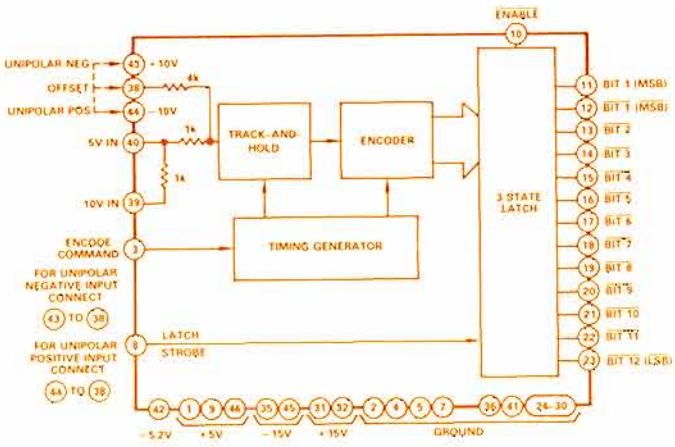
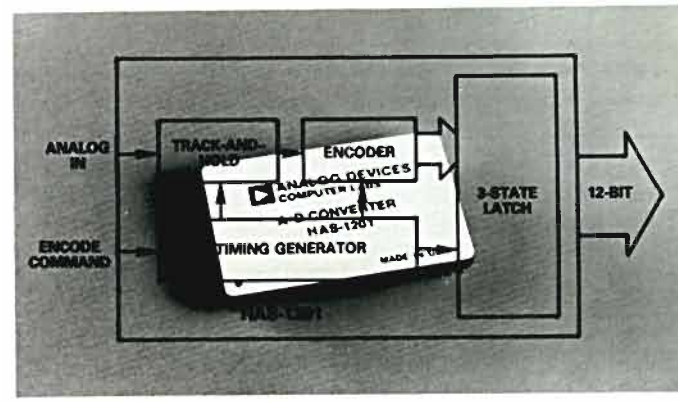


Figure 1. Functional block diagram of the HAS-1201



Designed for applications in radar, digital signal processing, medical instrumentation, and test systems, it eliminates the need for either a board-level product or a separate ADC and T/H.

Available in a 46-pin hermetically sealed metal package, the HAS-1201 linearity is typically within ½ LSB; monotonicity is guaranteed over temperature. The converter accepts bipolar or unipolar 5- or 10-volt signals, presenting respective input impedances of 1000 or 2000 ohms. Other dc specifications include 2-mV maximum input offset and 200 µV/°C max input offset drift.

In high-speed conversion applications, dynamic specifications are as important as dc performance. For the combined converter and T/H, the HAS-1201 offers typical 80-dB in-band harmonics and 67-dB signal-to-noise ratio (100-kHz input). The typical 3-dB signal bandwidth is 3 MHz for small signals and 500 kHz for large signals.

Outputs are coded in complementary: binary, offset binary, or twos complement; all outputs are TTL-compatible, and the output is interfaced to a 12- or 16-bit bus by a set of 12 parallel 3-state latches.

Standard supply voltages required are: +15 V, −15 V, +5 V, and −5.2 V, and power dissipation is 3.5 W max. Available in a 2.4″ × 1.6″ × 2″ (60 mm × 40 mm × 6 mm) hermetic metal package, the HAS-1201SM is specified over a −55°C to +100°C case-temperature range. The HAS-1201KM and HAS-1201SM are priced at $365 and $457 (100s).

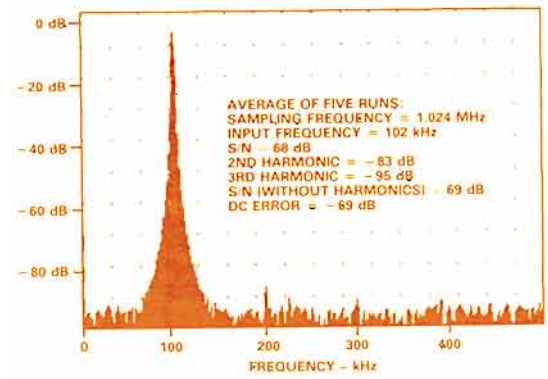


Figure 2. 512-point FFT spectrum of ADC output shows excellent harmonic and broad-band noise performance.

USE THE MONOLITHIC AD630 FOR PRECISION WAVEFORMS

Generate Square and Triangular Waves with Balanced Modulator/Demodulator Control Amplitude and Frequency Independently and Flexibly

by Walter G. Jung

A great many free-running relaxation oscillator circuits, employing R-C circuits for timing, have been published in recent years—including many that offer high precision.[1,2] Generally the precision of these circuits is restricted to their frequency predictability and stability; seldom do we see circuits that, in addition, offer accurate, easily adjustable output amplitudes.

The AD630* Balanced Modulator/Demodulator, described recently in these pages,[3] is uniquely suited for such applications, since it contains all the active circuitry needed to self-generate a square wave, with well-defined frequency *and* amplitude. To illustrate the device's versatility, we will describe here a precision astable circuit which has the flexibility to be modulated for transmitting data. We will also describe a function generator, which follows from the basic timing & control principles.

PRECISION ASTABLE OSCILLATOR

A square wave with predictable output amplitude can be built using a straightforward precision balanced modulator design, with a well-defined reference voltage as an input. The square-wave output can then be made to be equal to ± M times the reference voltage. We can generate the required timing signals for commutating the balanced modulator with a precision comparator—a function that is inherently available in the AD630.

In Figure 1, the AD630 is configured as a switched-gain amplifier, with alternate gains of +2 and −2, set by appropriate external pin-strapping of the device's internal precision feedback circuitry.

For gain of +2, when input A is active, the input (V_{REF}) is applied to A+, the non-inverting terminal of input A; and the gain is provided by feedback of ½ the output, via the two 10-kilohm resistors (there is no contribution by the 5-kilohm resistor, because both ends are at voltages equal to V_{REF}). When input B is active, the 5-kilohm resistor serves as an inverter input resistor, and feedback is via a 10-kilohm resistor, for a gain of −2 (the other 10-kilohm resistor is inactive because both ends are at 0 V). For best phase margin, the internal compensating capacitor (pin 12) is connected to the output terminal.

The timing characteristics of the circuit are defined by the feedback to the comparator, which switches the device inputs between A and B. There are two networks connected to the comparator inputs. To observe their function, let us suppose that the comparator has just switched to input A and the output is at $+2\times V_{REF}$. R1 and R2 provide a fixed positive feedback of ½ the output level (i.e., $+V_{REF}$), keeping the comparator positive and A in the circuit. At the same time, Rt & Ct develop an exponentially increasing voltage on Ct, at the negative input to the comparator, changing from its previous state ($-V_{REF}$) positively towards $+2\times V_{REF}$. When it reaches $+V_{REF}$, the comparator switches, V_{OUT} jumps to $-2\ V_{REF}$, and the exponential is now swinging back towards $-2\ V_{REF}$, with the next change of state occurring as it crosses $-V_{REF}$.

Referring to Figure 2, at the switching point,

$$+V_{REF} = -V_{REF} + 3\,V_{REF}\,(1-\epsilon^{-t/R_tC_t}) \quad (1)$$

$$1 = 3\epsilon^{-t/R_tC_t} \quad (2)$$

Since the circuit switches symmetrically, t is the half-period point

$$T/2 = t = R_tC_t \ln(3) = 1.1\,R_tC_t \quad (3)$$

$$f = 1/(2.2\,R_tC_t) \quad (4)$$

As with all oscillators with timing dependent on an R-C time constant, the predictability and stability will depend critically on that of the components used. Both should have low temperature coefficients; the resistor should be a metal-film type, and the capacitor should be a low-dielectric-absorption polystyrene or polypropylene film type. The most-predictable and accurate performance occurs below 10 kHz, but the oscillator is generally useful at

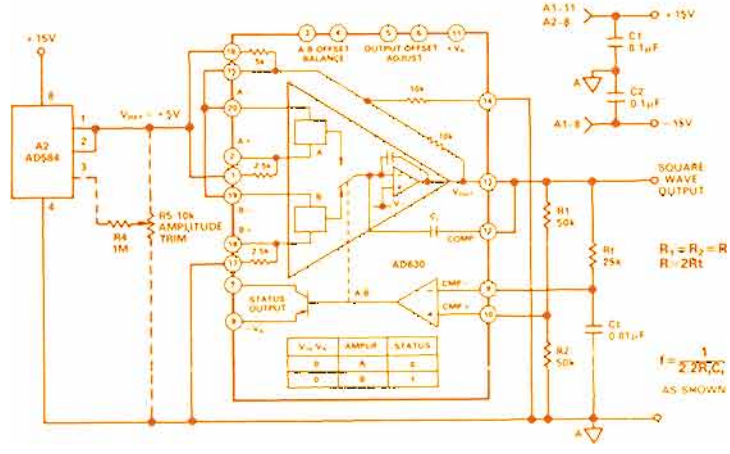


Figure 1. Precision astable oscillator.

*For technical data, use the reply card.

[1] Jung, W. G. *IC Op-Amp Cookbook Second Edition*. Indianapolis: Howard W. Sams & Co., Inc., 1980.

[2] —— *IC Timer Cookbook Second Edition*. Indianapolis: Howard W. Sams & Co., Inc., 1983.

[3] Brokaw, P., Gerstenhaber, M., Miller, S. "Fast, Flexible Switched Dual-Input Op Amp and Comparator." *Analog Dialogue* 17-1 (1983): 14-15.

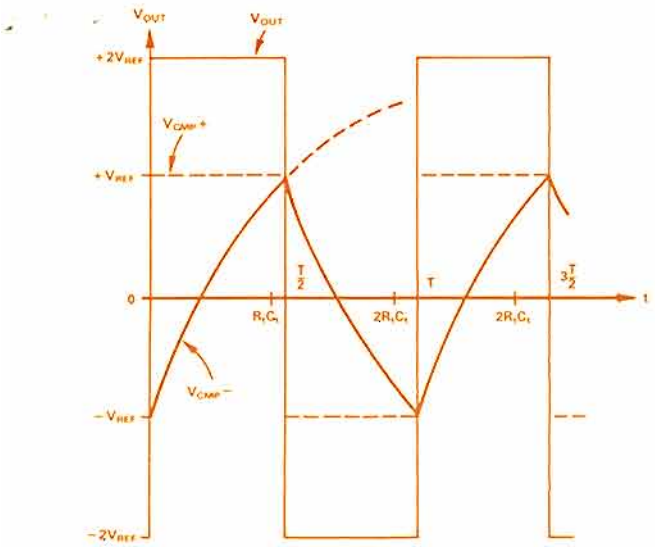


Figure 2. Waveforms illustrating operation of the circuit of Figure 1.

frequencies up to 100 kHz. In the example shown here, the frequency is approximately 1.8 kHz.

While the comparator's small switching window (±2 mV max over temperature) and fast action (200 ns step response time) enhance the predictability of the circuit's timing, the amplitude depends on the applied reference voltage, V_{REF}, and the gain-setting programmed into the AD630 (with gain error and mismatch less than 0.05%, when the internal resistors of the AD630BD or AD630KN are used). As it is set here, the peak output will be 2 V_{REF}, since the application resistors are strapped for gains of 2. The peak-to-peak output is, of course, 4 V_{REF}.

For V_{REF}, an AD584* precision reference-voltage source is used, with pins 1 and 2 strapped together for +5-volt output. Any alternative references used should have low output impedance, to minimize possible side effects which can arise from the dynamic load presented by the AD630's input when it is switched. This should not be surprising, since the AD630 responds to the comparator by essentially making two different op amp circuits available. The input impedance is characteristically high for the non-inverting mode and typically equal to R_A in the inverting mode.

With $V_{REF}=5$ volts and the gains equal to +2 and −2, an AD630AD (or JN) has a typical gain error of 0.1%. When it is used with an AD584K reference, the overall combined (untrimmed) amplitude tolerance will generally be less than 0.25%. For closer tolerances, the amplitude error can be reduced by the use of a trim network, shown in dotted lines in the figure.

Perhaps the principal virtue of the timing scheme employed can be seen in the step between equations (1) and (2): Since both the fraction of the output voltage and the amplitude of the exponential timing waveform are proportional to V_{REF}, the actual switching time, hence frequency, has a first-order independence of output amplitude. This basic scheme, made popular with the ubiquitous 555 timer[2], has an output frequency characterized by high immunity to output amplitude changes.

The practical advantage of this relationship is that the reference voltage can be programmed for different (coarse) amplitudes without disturbing the nominal operating frequency. Therefore you can strap the AD630, in this circuit, for different gains and output amplitudes, as well as different levels of V_{REF}, and the basic frequency relationship will remain the same.

While the main square-wave output of the AD630 is at an accurate ±10 volts, the STATUS output of the AD630's comparator—also a square wave—is available at pin 7. This output can be used for external synchronization and interfacing to logic operations. It is an NPN open collector, capable of swinging between ±15 volts.

MODULATED OSCILLATOR

The astable circuit described above, using the AD630, can maintain oscillation while, at the same time, it is being amplitude modulated. If an a-c or slowly varying d-c signal is summed with the output of the reference source and applied as a composite input to the AD630 oscillator, a very linear amplitude modulator (AM) results. Figure 3 shows a modification to the reference circuit that will accomplish this form of modulation.

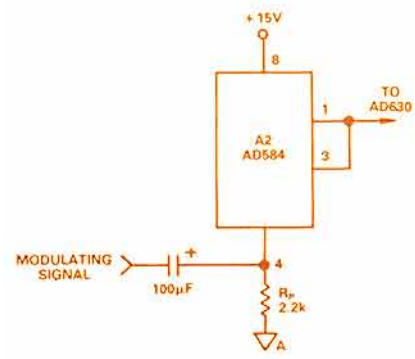


Figure 3. Input modification for amplitude modulation.

In this circuit, the AD584, connected for 2.5-volt output, is also used as a current source, developing a dc voltage across R_p. The ac-coupled modulating signal is added to the dc bias appearing across R_p, and the AD584 buffers it to provide a low-impedance output, shifting it by +2.5V. The total V_{REF} applied to the AD630's input will be the basic output of the AD584 plus the ac and dc voltages across R_p. Since the AD630 in effect multiplies its input alternately by +2 and −2, at the carrier frequency, the effect is to provide an amplitude-modulated waveform.

Figure 4 shows the performance of a test circuit using this scheme, employing a 20-Hz modulating signal and a 93-Hz carrier. The upper waveform is the output of the modulated oscillator, while the lower one is the 20-Hz signal recovered at the output of a second AD630, connected as a synchronous detector,[3] with the signal output of the first AD630 connected to both the signal and the synchronizing inputs. Even without low-pass filtering to remove residual carrier components, the total harmonic distortion at a 2-volt rms level is less than 0.1%.

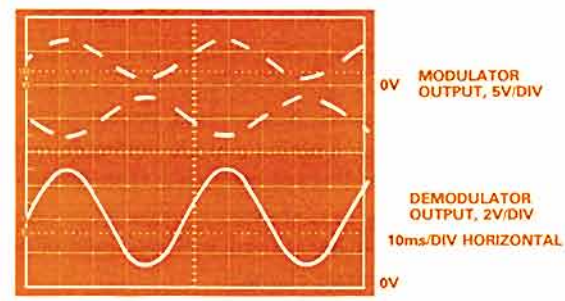


Figure 4. Amplitude-modulated oscillator waveforms. Upper: modulated waveform. Lower: Recovered waveform.

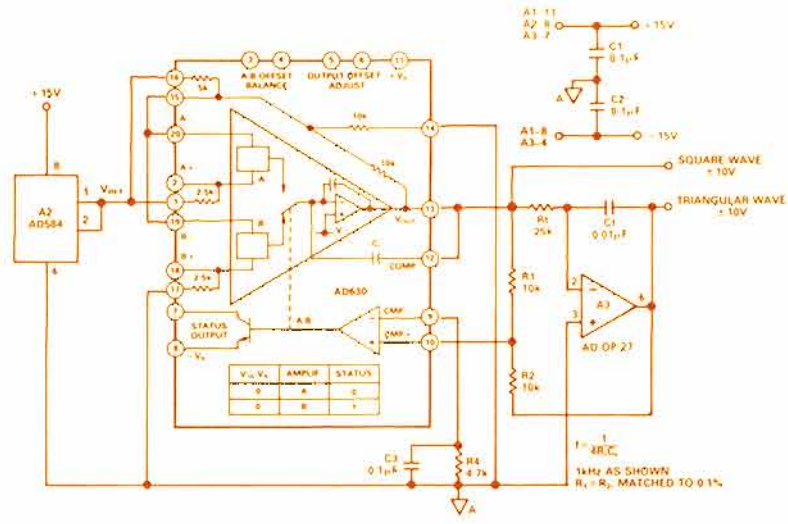


Figure 5. Precision triangular-wave and square-wave function generator.

FUNCTION GENERATOR

Quite often there is a need for precise and stable triangular waveforms, for example in linear crossplotting and in trigonometric function circuits. With relatively small changes, the circuit of Figure 1 can be easily adapted to this type of application.

If a linear integrator output, instead of a passively generated exponential, is used as the timing element in the feedback circuit, the same kind of symmetrical square-wave can be generated, but in addition, the integrator output will be a linear triangular wave (Figure 5). By proper choice of R_t and C_t, its peak-to-peak amplitude can be precisely set at (say) 20 volts.

To implement the integrator function, amplifier A3 is used in a conventional integrator circuit. A low-offset, low bias-current, high gain-bandwidth op amp is best for this application, for example, the AD OP-27. With equal comparator input-resistors, and a ground reference at the comparator's negative input, the integrator will produce linear ramps, symmetrical about ground. For a triangular-wave swing of 4 V_{REF} to be generated each half-period, while the integrator's input magnitude is equal to 2 V_{REF}

$$R_tC_t = 1/(4f) \qquad (5)$$

The comparator crossings occur when ½ the triangular-wave output voltage is equal to V_{REF}, i.e., when the peak value is equal to 2 V_{REF}.

In the example shown, R_t and C_t are chosen for a 1-kHz operating frequency. In this version, the general limitations on operating frequency are similar to those for the astable circuit with passive timing. The circuit is useful up to tens of kHz, but the best predictability and timing precision occur below a few kHz. For frequencies less than 1 kHz, the predictability of this circuit is excellent; in fact, it is limited by the components used for R_t, C_t, R_1, and R_2.

With components of appropriate precision for the resistances, you can even use the circuit as a high-resolution capacitance-measuring tool, by measuring the oscillator period, since period is directly proportional to C_t. With a period counter with 6 or more digits of resolution, this allows direct plug-in capacitance measurements. The resolution and stability of the circuit are such that capacitance differences of 10 ppm can be resolved, with high immunity to both reference- and supply-voltage changes.

As a general-purpose function-generator circuit, there are a number of useful modifications available. The operating frequency can be made programmable, either by analog switch selection of the R_t value (for programming coarse increments) or by inserting a multiplying CMOS DAC-plus-amplifier combination ahead of the A3 integrator stage (for fine-increment programming). A logarithmic DAC can be used for programming in logarithmic steps, but care should be taken (by switching integrator time constants) to minimize drift errors at low frequencies.

When the DAC-programming approach is used, another sign inversion usually occurs in the control loop. This calls for *differential* sensing at the comparator input, in the manner of Figure 1. It is accomplished by removing $R_4 - C_3$ and disconnecting R2 from R_1/pin 10 and re-connecting it to pin 9 of the AD630. There will be no scale change.

With the function-generator frequency programmable via a CMOS DAC, there are some additional constraints to consider. The DAC-plus-amplifier is inside the frequency-determining loop and periodically hit with a fast square wave from the AD630. Any dynamic problems, for example, high capacitance, or asymmetrical response, will reduce overall performance. For many of the older CMOS DAC types, while the circuit operates to well above 1 kHz, the linearity constraints do not allow full 10-bit accuracy to be attained, as is possible at lower frequencies. Use of the newer, lower-capacitance DACs, such as the AD7240, will be helpful.

On the upside, however, bus-compatible latched DACs make possible fully programmable function generation, with both frequency and amplitude under microprocessor-control. For applications calling for manual control, such conveniences as log-taper manual pots allow a wide range of manual frequency control. Three or more decades of control without serious loss of waveform symmetry is possible, since A3 is a low-offset device and can integrate millivolt input levels.

SUMMARY

The AD630, a precision balanced modulator/demodulator, allows very high-precision RC timing circuits to be implemented at low to medium frequencies, with easy control of amplitude. When it is used with dc control signals, the output voltage level is as precise (0.05% to 0.1%) as the reference voltage source used to define the amplitude limits, a characteristic difficult to implement with other circuit approaches. When it is used within integrator-loop function-generator circuits, precise triangular-wave amplitudes are available, because of the device's on-chip precision comparator.

FLEXIBLE MONOLITHIC INSTRUMENTATION AMPLIFIER

AD625C Has 0.001% Max Nonlinearity, 5 ppm/°C Max Tempco, 4 nV/√Hz RTI Noise

Gains Are Programmable by Choice of External Resistors or by Software

by Scott Wurcer

The AD625* is a high-performance instrumentation amplifier fabricated on a single monolithic chip. It is a second-generation member of the family of IC instrumentation amplifiers introduced in 1982 by the AD524[1] and, more recently, the AD624[2]. It is characterized by ultra-low nonlinearity (10 ppm max), 25 μV max input offset voltage, 2 mV max output offset voltage, and a minimum of 120 dB common-mode rejection, (all for the AD625C).

The AD625 differs from its predecessors in one important respect. While they contain sets of resistors with laser-trimmed ratios for convenient pin-programming of preset gains, the AD625 has the increased flexibility available with the use of *external gain resistors*. This is important in two ways: gain settings can be switched without regard to switch resistance; and the user can choose any desired set of gains, from 1 to 10,000. Thus, the AD625 can be used as a software programmable-gain amplifier with arbitrary choice of gains, using low-cost CMOS multiplexers for gain switching.

In addition, since the maximum gain error is 0.02% (with a max gain tempco of 5 ppm/°C), the external precision resistors may be specified for the desired gains and installed directly, without requiring gain trims or calibration in most applications.

Performance is excellent, even for the lower-cost grades: the AD625A has max specs of ±0.005% nonlinearity, ±0.05% gain error, 200 μV input offset voltage, 5 mV output offset voltage, and 110 dB min of common-mode rejection, with noise and dynamic specs similar to those of other grades. The AD625 is available in a 16-pin ceramic DIP and is specified over a −25°C to +85°C temperature range for the A, B, and C grades, and −55°C to +125°C for the S grade. Prices in 100s for A/B/C/S are $9.50/$13.50/$22.50/$27.00.

HOW IT WORKS

The basic principle of operation of the AD625 was described in (1). Essentially, the AD625's circuit is a variation of the classical "3-op-amp" instrumentation amplifier circuit (Figure 1). The differential input voltage ($V_{in} = V^+ - V^-$) is duplicated across a pair of "gain sense" terminals, which are connected to a resistor, R_g. The current through R_g (equal to V_{in}/R_g) is furnished through a pair of feedback resistors, R_{f1} and R_{f2} from the outputs of the two input amplifiers, which must be at the correct voltages to adjust the voltage across R_g to precisely equal V_{in}.

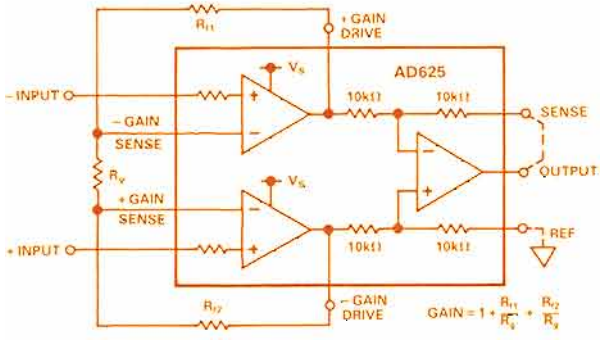


Figure 1. Basic application of the AD625 – functional diagram.

The output amplifier is simply a unity-gain subtractor; its purposes are common-mode rejection—to bring the output level down to the output reference level—and to provide a low-impedance output range of ±10 V at 5 mA.

The expression for gain is

$$G = 1 + R_{f1}/R_g + R_{f2}/R_g \quad (1)$$

or, if $R_{f1} = R_{f2} = R_f$,

$$G = 1 + 2R_f/R_g \quad (2)$$

Dynamic performance is excellent. An important virtue of the AD625's input circuit is the increase of input-circuit transconductance as R_g is reduced (and the gain is increased). This tends to slow the decrease of bandwidth as gain is increased; the small-signal −3 dB bandwidth is 650 kHz at unity gain, 100 kHz at gain of 100, and 25 kHz at gain of 1000 (gain-bandwidth of 25 MHz). The slew rate is 5 V/μs, and 0.01% settling-time ranges from 15 μs (for gains up to 200) to 75 μs at G = 1000.

Figure 2 shows an application in which a choice among three digitally set gains, 4, 16, and 64, is established by 7 resistors and 3 pairs of switches. If a dual 4-channel multiplexer, such as the AD7502, is used, a fourth gain could be added, using an additional pair of resistors. Note that no signal current flows through the switches, hence gain is independent of switch resistance; at worst, bias current flowing at the gain-sense terminals may produce a small offset voltage in the resistor string.

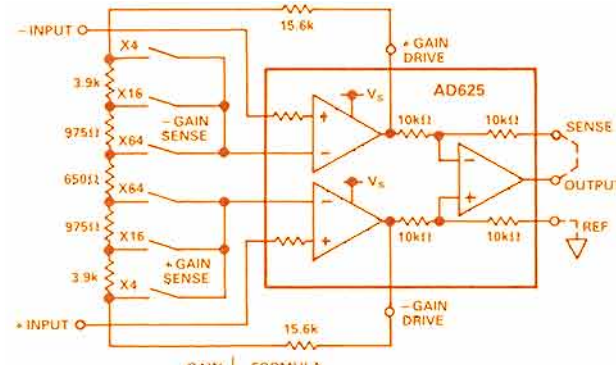


Figure 2. Programmable-gain application: 4, 16, 64

*Use the reply card for technical data.

[1]Wurcer, S. and Gerstenhaber, M. "Analog Signal-Conditioning ICs Take Two Giant Steps," *Analog Dialogue* 16-3 (1982): 3-6.

[2]"Unparalleled Instrumentation Amplifier," *Analog Dialogue* 17-3 (1983): 24 (New-Product Brief).

THERMOCOUPLE-BASED SETPOINT CONTROLLERS

AD596 & AD597: Monolithic Thermocouple Instrumentation Amplifiers in TO-100 Can Provide Ice-Point Compensation, Setpoint, and On-Off or Proportional Output

The AD596* and AD597*, the industry's first thermocouple-based monolithic setpoint controllers, offer a cost-effective solution to temperature measurement and control. Each accepts a thermocouple output, amplifies it, and compares it to a voltage signal representing a temperature setpoint. When the thermocouple output exceeds the setpoint, the AD596/AD597 output switches from low to high—and vice versa; this high/low signal can be used to control a relay to switch a heating element off or on.

The AD596 and AD597 each contain an on-chip instrumentation amplifier, cold-junction compensation, comparator and open-thermocouple-alarm circuits. The AD596 accepts millivolt-level signals from a J-type thermocouple (iron-constantan) to measure temperatures from −200°C to +750°C, while the AD597 accepts millivolt-level signals from a K-type thermocouple (chromel-alumel) to measure temperatures from −200°C to +1,250°C.

Their cold-junction compensation circuit provides, in effect, the specified ice-point (0°C) reference for the active thermocouple junction without regard to the AD596/AD597's actual ambient temperature. The temperature signal is amplified to have a sensitivity of about 10 mV/°C and is compared to the setpoint voltage, which can be generated by a d/a converter or a potentiometer and voltage reference. The user can provide an adjustable deadband, by means of an external resistor, to reduce the rate of "hunting" about the set point.

The AD596/AD597 operate with a single +5-volt supply and are specified for accurate operation (±4°C maximum absolute error at 60°C ambient, with 0.05°C/°C max ambient temperature rejection) over a range of ambient temperatures from +25°C to +100°C; they are thus optimized for operation in higher-temperature ambient environments. Both are packaged in hermetically sealed 10-pin metal TO-100 cans.

In addition to being complete and self-contained, the AD596 and AD597 are identically low-priced; they can reduce system component count and assembly cost, thus reducing the cost of designing temperature controllers for appliances and commercial, residential, and industrial equipment. Price of either unit in 10,000's is only $5.00.

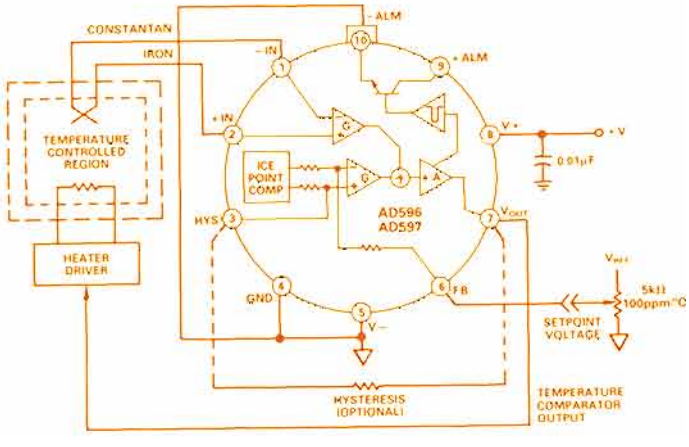
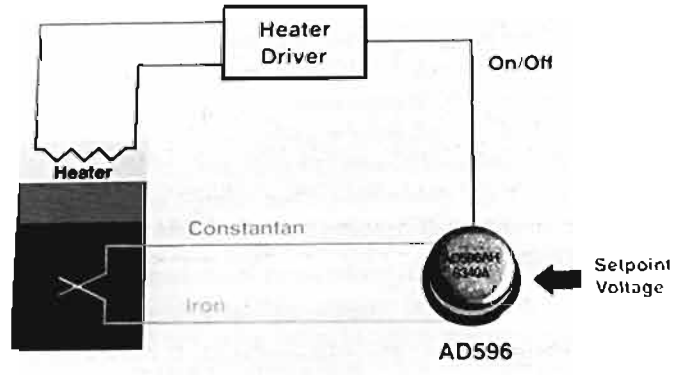


Figure 1. The AD596 as an on-off controller.



They have an open-thermocouple detection circuit, which signals a break in one or both of the thermocouple leads; this feature is of critical importance in applications where such fault conditions can trigger an inappropriate system response. The open-thermocouple output can trip a microprocessor interrupt or drive an LED indicator on an instrument panel.

Figure 1 is an on-off temperature-control application, which also shows a functional block diagram of its basic internal circuit. You can see that, inside the device, the thermocouple output is amplified and summed with the ice-point compensation and the set-point voltage, in appropriate polarity; and the open-loop high-gain amplifier, A, acts as an on-off comparator.

Figure 2 shows a measurement application, with output voltage proportional to thermocouple voltage, at a sensitivity of about 10 mV/°C. Here, the feedback loop has been closed, via pin 6; the amplifier functions as a conventional closed-loop linear amplifier instead of as an open-loop comparator.

The AD596/AD597 will also function as a stand-alone ambient temperature-measuring circuit.

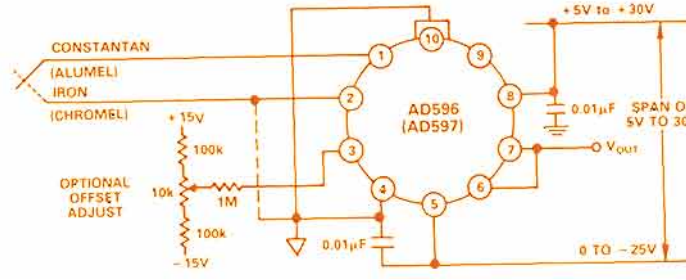


Figure 2. Linear thermocouple-output measurement.

AUTORANGING μP-BASED RTD/THERMISTOR METERS

AD2060/AD2061 Self-Calibrate Gain, Offset & Excitation, and Linearize Data

Character-Serial ASCII Output; Optional Analog, Serial TTL & Isolated 20-mA Loop

The AD2060 and AD2061* are high-performance single-channel 3 ½-digit temperature meters designed for RTD or thermistor inputs. Both meters can measure temperature accurately between −328°F and +1562°F (−200°C and +850°C); the meters automatically select the correct gain range to provide resolution of 0.1° (F or C) for temperatures between −199.9° and +199.9°, 1° for magnitudes of 200° or more. In addition, the on-board microprocessor provides automatic calibration of gain, offset, and excitation, as well as linearization of the measured temperature.

Sensor	Range	Accuracy
100Ω RTD, α = 0.00385	−200°C to +850°C	±0.3°C ± 1/2LSD
	−328°F to +1562°F	±0.6°F ± 1/2LSD
100Ω RTD, α = 0.00392	−200°C to +640°C	±0.3°C ± 1/2LSD
	−328°F to +1184°F	±0.6°F ± 1/2LSD
100Ω RTD, α = 0.00390	−200°C to +640°C	±0.3°C ± 1/2LSD
	−328°F to +1184°F	±0.6°F ± 1/2LSD
Thermistor, R = 2252Ω	−30°C to +100°C	±0.4°C ± 1/2LSD
	−22°F to +212°F	±0.8°F ± 1/2LSD

Table 1. Readout accuracy (at 25°C ambient).

The *AD2060* is programmed at the factory for one of four sensor types: 100-ohm 2, 3, or 4-wire platinum RTDs with α of 0.00385, 0.00390, or 0.00392, and Series 400 thermistors, R = 2252 ohms. The *AD2061* is a universal device, switch-programmable by the user for any of the above sensors. Table 1 illustrates the accuracy of the meters with the various sensors.

Typical applications include monitoring of temperature in laboratory, manufacturing, and quality-control environments, process-control temperature measurements, and remote data logging. Choice of °F/°C is made by the user via a selector switch behind the lens.

Temperature information is displayed on large 0.56"H (14.3 mm) LEDs. As Figure 1 shows, it is also available digitally in character-serial ASCII format with rate selection (25 or 100 characters per second) for easy interface to printers, terminals, and other peripherals. Options for computer interfacing include an isolated (600V) 20-mA bit-serial loop output—capable of 300 or 1200-baud operation over distances up to 10,000 feet—and a non-isolated TTL-compatible interface.

Linearized temperature information is also optionally available in analog form as a 1 mV/° output voltage for driving recorders and other analog instruments.

The operating ambient temperature range for specified operation of these meters is 0°C to +40°C with range temperature coefficients of 20 ppm/°C typical, 30 ppm/°C maximum. You can order either meter for nominal power supplies of 120 V ac, 240 V ac, or +7.5 to +28.0 V dc. The meters automatically indicate over-range and open-sensor conditions. They are protected for 180-volt peak input (RTD short to ac line) and common-mode voltage to 1,400 V peak (ac-operated versions).

Before shipment, all devices are burned in for 168 hours at 50°C, power-on-off cycled, and calibrated (traceable to the National Bureau of Standards). The meters are supplied in rugged molded plastic cases that meet UL94V-0 and DIN/NEMA standard dimension requirements. Base prices of the AD2060/AD2061 are $295/$355 (1-4) and $206.50/$248.50 in 100s.

*Use the reply card for technical data.

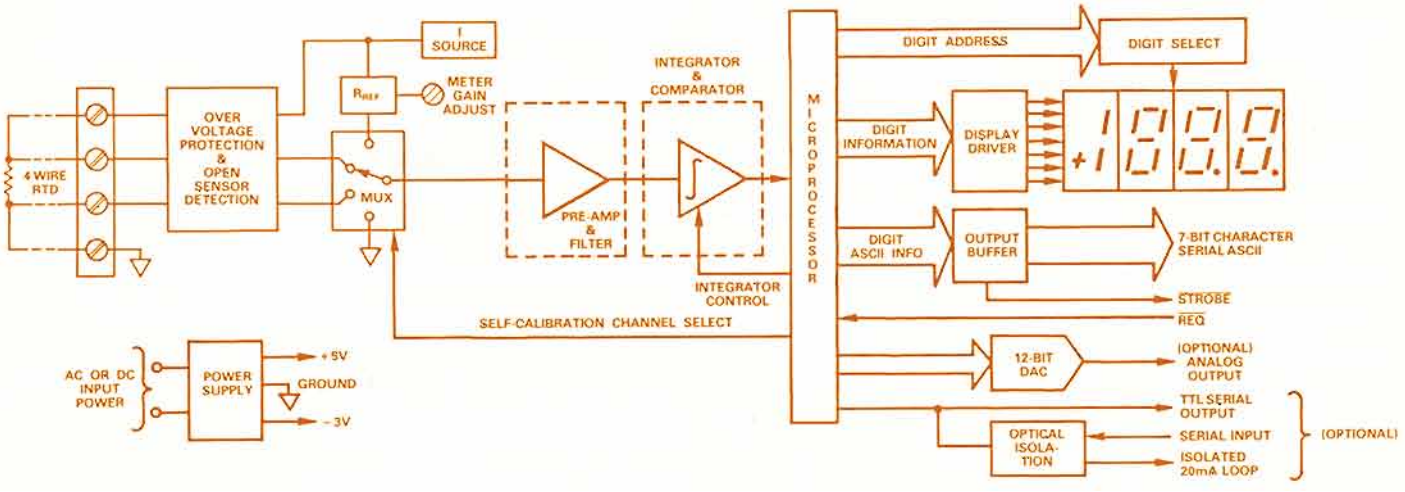


Figure 1. Functional block diagram of the AD2060 & AD2061.

NEW HYBRID RESOLVER-TO-DIGITAL CONVERTER FAMILY

1S20/40/60/61 Tracking-Type Converters Offer 12-, 14-, & 16-Bit Resolutions For Position Measurement in Numerical Machine-Tool Controls and Robotics

by John Gasking

The 1S20/40/60/61* are a pin-compatible family of compact, low-cost hybrid resolver-to-digital converters (using a 32-pin triple-DIP package) designed for applications requiring 12/14/16/16-bit resolution. Designed to have high tracking rates and to make available all the essential features needed for numerically controlled machine-tool applications they are equally useful in robotics. In addition, their capabilities make them desirable wherever rotary or linear position measurements are desired, whether in windmills, antennae, or satellites.

Because of their ruggedness, reliability, isolation, and immunity to noise, resolver systems using these completely self-contained converters are ideal for supplanting incremental and absolute encoders, as well as phase-analogue and sampling (peak-follower) type converters. In addition, the low prices of these devices should tend to discourage the in-house design of converters—which often appear to have low parts cost, but are nevertheless more expensive if the hidden costs due to essentially "re-inventing the wheel": complexity, unknown reliability, and testing, are forthrightly taken into account.

BRIEF REVIEW OF RESOLVERS

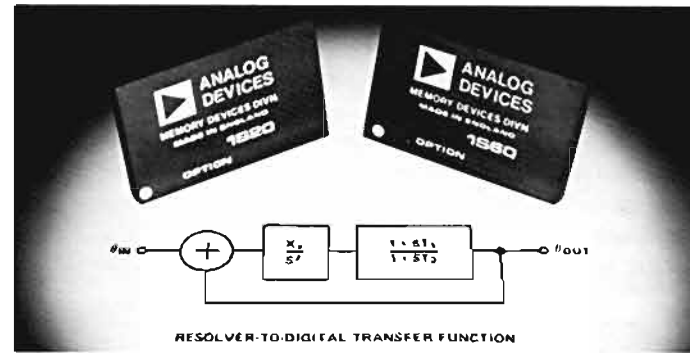
A resolver is a rotating transformer whose output analog voltages are uniquely related to its shaft angle. It can measure angular positions within 0° to 360° of rotation. An Inductosyn† is a printed-circuit resolver that can be laid out flat on plane or cylidrical surfaces for direct linear or rotary measurement; when its millivolt-level output is amplified, it can be treated electrically in the same way as a resolver.

A resolver has three sets of windings: two stator windings at right angles, and a rotor winding. There are two ways to use it: drive the stator windings electrically at 90° and measure the electrical phase angle of the rotor, or drive the rotor winding, measure the amplitudes of the stator voltages (proportional to the sine and cosine of the angle), and compute the arctangent of their ratio.

Although the first method may look simpler, practical implementation schemes tend to be sensitive to electrical noise; on the other hand, the second method has an easy implementation when combined with a tracking analog-to-digital conversion scheme—and it is insensitive to reference amplitude and noise. A further bonus is that a velocity signal is available for use in control loops. Since a resolver is a transformer, the ratio of output to reference is simply the transformation ratio, independently of amplitude; though a maximum rating is specified (e.g., 26 V) resolvers work well when delivering 2-volt output signals in angle measurement.

The 1S20/40/60/61 series use the latter method (Figure 1). The sine and cosine signals are applied to the signal input,

$$V_1 = K E_0 \sin \omega t \sin \theta$$
$$V_2 = K E_0 \sin \omega t \cos \theta \qquad (1)$$



RESOLVER-TO-DIGITAL TRANSFER FUNCTION

where θ is the angle of the resolver shaft or the fractional distance through a particular pitch of the Inductosyn.

The up/down counter stores the present value of the digital angle, ϕ. Its sine and cosine are multiplied by the resolver outputs

$$K E_0 \sin \omega t \sin \theta \cos \phi$$
$$K E_0 \sin \omega t \cos \theta \sin \phi \qquad (2)$$

and subtracted by the error amplifier to give

$$K E_0 \sin \omega t \sin (\theta - \phi) \qquad (3)$$

These elements and a phase-sensitive detector, integrator, and voltage-controlled oscillator (VCO) form a closed-loop system, which seeks to null the difference between shaft angle, θ, and the reconstructed digital angle, ϕ, by incrementing the counter appropriately. When this is done, $\phi = \theta$, to within the rated accuracy of the converter. *Direction* and *ripple clock* outputs allow simple extension counters to implement multi-pitch ($< \pm 360°$) operation.

The outputs of the 1S20/40/60/61 form a left-justified 16-bit word, which may communicate with an 8- or 16-bit data bus via high- and low-byte enable controls. There are three frequency options for each model, giving speeds up to 170/42.5/10.5/10.5 revolutions per second. Repeatability is to within 1 LSB (1.5 arc-min over temperature) and accuracies are to ±8.5/5.3/4.0/10 arc-min over temperature—and for variations of up to 10% in signal and reference amplitude, frequency, and harmonic distortion. Prices of the 1S20/40/60/61 in 100s are $107/$119/$201/$113.

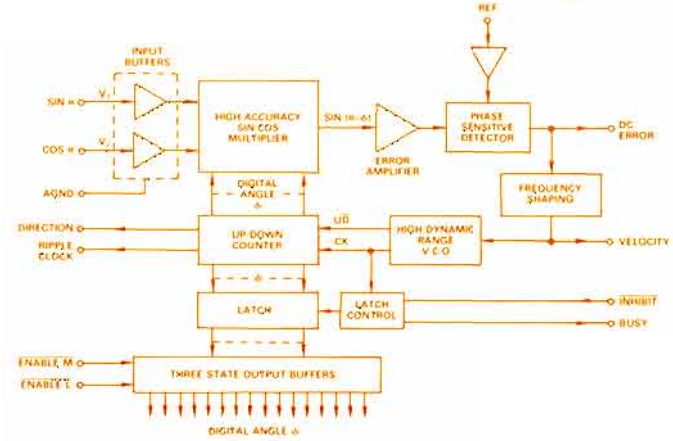


Figure 1. Functional diagram of tracking resolver-to-digital converter.

*For technical data, use the reply card.
†Inductosyn is a registered trade mark of Farrand Controls, Inc.

LOW-COST 12-BIT ANALOG INTERFACE BOARDS FOR VME BUS

Expandable RTI-600 Analog Input Board: 16 Single-Ended/8 Differential Inputs

RTI-602 Output Board Has 4 Voltage Outputs and Optional Current-Loop Outputs

The RTI-600 and RTI-602* bring low-cost analog input and output capabilities to VMEbus microcomputers. Available in the single Eurocard format (100 × 160 mm), these boards provide a versatile analog to VMEbus interface for a wide range of applications in laboratories and in factory automation and product test.

The RTI-600 Analog Input Board (Figure 1) offers 16 single-ended or 8 differential input channels, expandable to 32 single-ended or 16 differential channels. An on-board instrumentation amplifier, with user-selectable gains from 1 to 1,000, permits direct connection of low-level signals. The 12-bit analog-to digital converter (AD574*) offers accuracy to within ±0.01% and unipolar or bipolar input ranges of 0 to +10 V or ±10 V, with conversion rates of up to 25,000 channels per second. The input channels have 78 dB of common-mode rejection, common-mode voltage range of ±10 volts minimum, and protection against overvoltage.

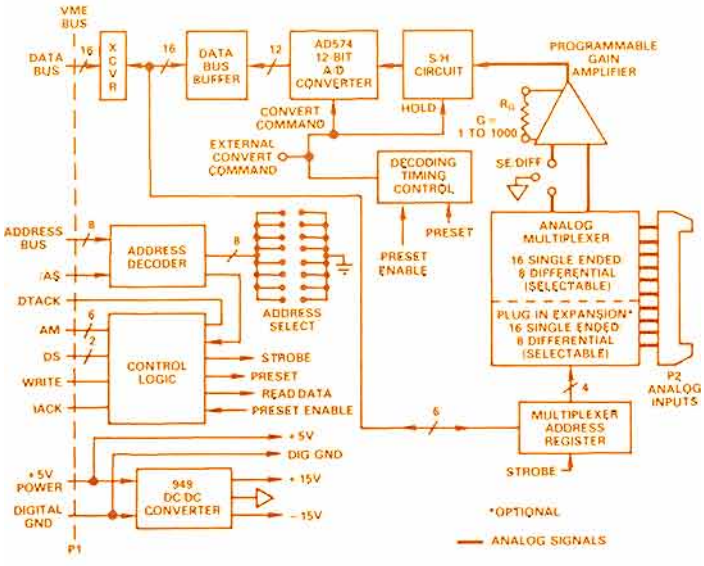
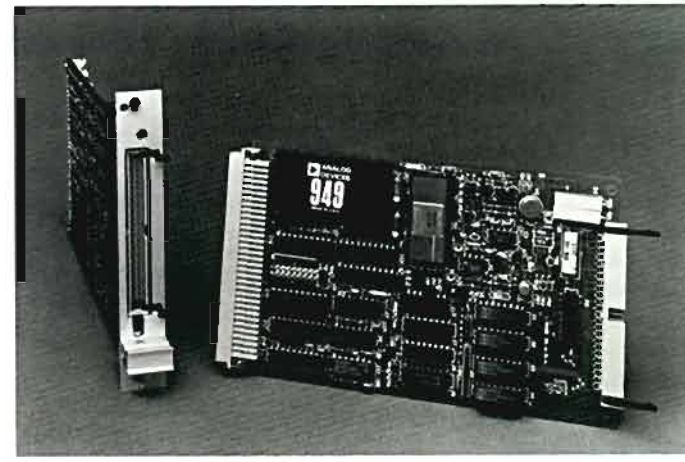


Figure 1. Functional schematic of RTI-600 Analog Input Board.

The RTI-602 Analog Output Board (Figure 2) offers 4 analog output channels, each with 12-bit resolution (AD7541*). Output voltage ranges include: 0 to +5 V, 0 to +10 V, ±5 V, and ±10 V. The board contains an option for two 4-to-20 mA current outputs. Other typical specifications include ±½-LSB nonlinearity, 25-µs settling time to ±½ LSB, and gain error of ±0.01% of full scale.

For sensor-based applications, where direct connection to the sensors and front-end signal conditioning are necessary, the RTI-600 and RTI-602 connect directly to Analog Devices 3B-series signal-conditioning manifolds.

The 3B *input* modules provide ±1500-volt isolation, 130-volt ac input protection, amplification, and filtering; they are designed for direct screw-terminal connection of low-level signals from transducers, such as thermocouples, strain gages, and RTDs. The 3B *output* modules make isolated and non-isolated voltage and current channels available to the RTI-602's outputs. For external wiring, the RTI boards use an IDE pin-and-socket connector with latching header. This feature ensures the integrity of sensor-wiring connections under mechanical stress or vibration.



The RTI-600 and RTI-602 are memory-mapped into the VME short I/O address space and are compatible with all VME CPU-boards, interfacing through the primary connector (P1). Both of these boards contain an on-board dc-to-dc converter, which provides the correct voltages to power the analog circuitry, starting with standard +5-volt computer power. Operation is specified over the 0°C to +70°C range. In 25-piece lots, the RTI-600 and RTI-602 are priced at $535 and $411.

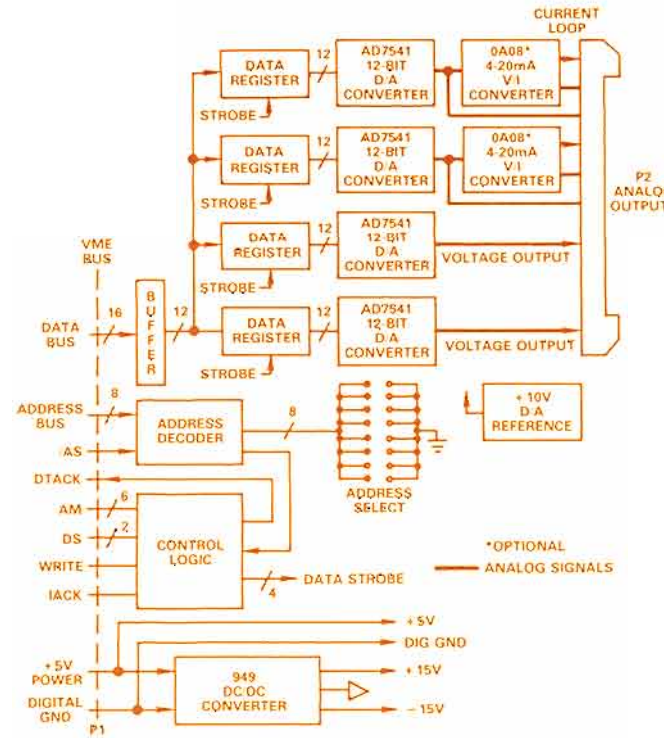


Figure 2. RTI-602 Analog Output Board.

*For technical data, use the reply card.

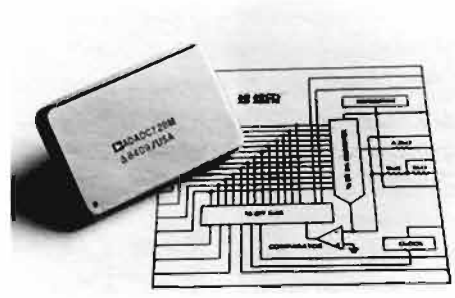
16-BIT HYBRID A/D CONVERTER

Improved AD ADC71/72C Have Existing Second Sources
Lower Chip Count and Dissipation for Higher Reliability

The AD ADC71 and AD ADC72* are complete 16-bit hybrid analog-to-digital converters in hermetically sealed 32-pin triple-width dual in-line packages. They are designed conservatively for high performance in order to meet industry-standard specifications readily with high manufacturing yields and low cost. Additional factors tending towards improved performance and increased reliability for the AD ADC71/72 are the lower chip count and reduced power dissipation.

The AD ADC72 is hermetically sealed in a metal package and available for operating temperature ranges of 0°C to 70°C & −25°C to +85°C; the non-hermetic AD ADC71, at lower cost, is available for the 0°C to 70°C temperature range. Prices start at $140.00.

Like its industry peers, the AD ADC71/72 have 16-bit resolution, with two options for guaranteed no-missing-codes: to 13 bits (0°C to 50°C, J and A grades) and to 14 bits (10°C to 40°C, K and B grades).



Salient features include ±0.003% maximum nonlinearity (K and B grades), fast conversion (45 μs to 14 bits), short-cycle capability for faster conversion, and TTL-compatible parallel or serial data outputs with corresponding clock and status outputs.

Their small size, 16-bit resolution, and 14-bit accuracy make these devices useful wherever high-resolution a/d conversion is necessary, including automatic test equipment, medical instrumentation, multi-channel conversion of signals with diverse dynamic ranges, and industrial robotics.

FET OP AMP

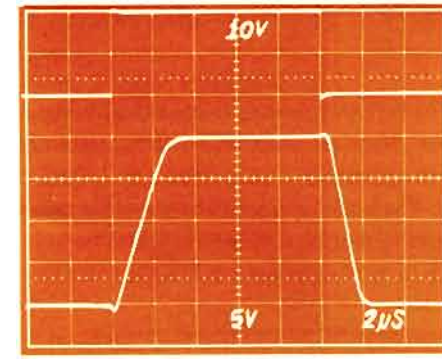
AD611 Lowers Design Cost of High-Precision Circuits

The AD611* is a drift-trimmed monolithic field-effect-transistor-input op amp employing an implanted FET process. Housed in a hermetically sealed TO-99 package, it is designed to offer premium performance at highly competitive prices.

It is available in two grades; highest performance is provided in the AD611KH, with max offset voltage of 0.5 mV, max offset tempco of 10 μV/°C, and max bias current (25°C, fully warmed up) of 50 pA. Comparable specs for the AD611JH are 2.0 mV, 20 μV/°C, and 100 pA. Prices (100s) for AD611JH/KH are a low $1.00/$1.95.

In addition to the excellent dc specifications, the design of the AD611 is optimized to deliver a 13 V/μs slewing rate, 2-MHz unity-gain bandwidth, and settling time—to 0.01%—of 3 μs.

This combination of performance makes the AD611 ideal for any FET application where excellent performance at low cost is required. Its wide bandwidth, low offset voltage, and fast settling time make the device ideal as an output amplifier for current-output d/a converters of all types. The illustration shows the large-signal (20-volt step) response of a CMOS DAC in the 4-quadrant multiplying mode, employing an AD7533 with AD611's as output op amps.



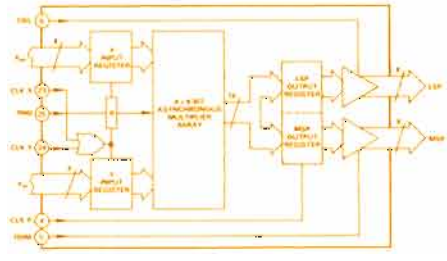
80 dB of common-mode rejection and 94 dB of open-loop gain ensure "12-bit" performance in high-speed buffer circuits. Its excellent noise performance at low frequency, as well as its low supply-current requirement, will benefit any general-purpose BIFET application.

8 × 8 MONOLITHIC CMOS MULTIPLIER

ADSP-1081 Dissipates 100 mW, Multiplies in 75 ns
Unsigned Format Simplifies One-Quadrant Multiplication

The ADSP-1081* is a TTL-compatible 8-bit × 8-bit monolithic CMOS digital multiplier that is pin-for-pin compatible with the MPY-8HUJ but demands an order-of-magnitude less power. A fast multiplier, the ADSP-1081 performs a clocked multiplication in less than 90 ns over the commercial temperature range (KD grade), less than 105 ns over the −55°C to +125° *ambient* temperature range (TD), and only 75 ns, worst case, at 25°C.

The ADSP-1081 is designed for unsigned, one-quadrant multiplications. This means that it, unlike the 8 × 8 ADSP-1080 (which has a twos-complement data format), provides one or two bits of additional precision for unipolar data without external shifting (important at the 8-bit level), because sign



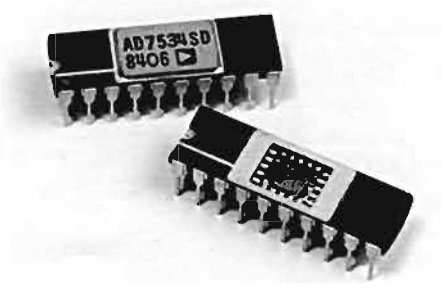
bits aren't required. The output, a double-precision product, is compatible with 8- and 16-bit data buses.

Typical applications for the ADSP-1081 are in digital signal processing (filtering and Fourier transforms), digital image processing, matrix multiplications, and microprocessor acceleration. Prices start at $31.00 (ADSP-1081JD, in 100s).

*Use the reply card for technical data.

14-BIT CMOS DAC

Monotonic Over Temperature
Double-Buffered Inputs



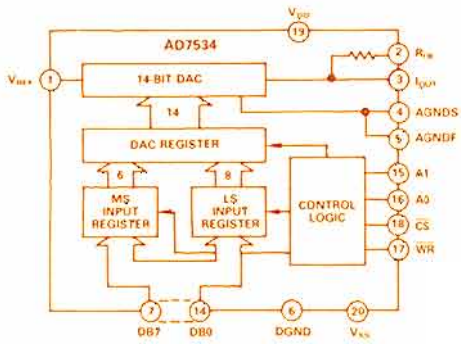
The AD7534* is a µP-compatible 14-bit multiplying digital-to-analog converter in a 0.3" 20-pin dual in-line package. It owes its small size and high performance to the use of the Analog Devices LC²MOS (Linear-Compatible CMOS) process, thin-film resistors and laser-wafer trim, and a novel low-leakage configuration (patent pending).

All grades of the AD7534 have differential nonlinearity less than ±1 LSB and are 14-bit monotonic over the full temperature range. Relative accuracy error is ±1 LSB max and full-scale gain error is ±4 LSB max (grades K/B/T, over temperature). Gain tempco for these grades is ±2.5 ppm/°C max, with typical tempco of 0.5 ppm/°C.

Typical applications are in µP-based control systems, reconstruction in digital audio, and high-precision servo control.

Fully microprocessor-compatible (TTL/5-V CMOS logic), the device can accept right-justified data in two bytes from an 8-bit bus and is double buffered to permit simultaneous update (as well as independence between loading from the bus and updating of the analog signal).

Prices start at $16.95 (AD7534J in 100s).



*For technical data, use the reply card.

A-D "EYE": INTELLIGENT VISION SYSTEM

Low-Cost Automated Inspection and Robotic Vision
Gray-Scale Capability Minimizes Lighting Constraints

Analog Devices has announced its entry into machine-vision with the IVS-100 Intelligent Vision System*, to be described at greater length in a future issue of *Dialogue*.

The IVS-100 is a system for processing images acquired from one or more television cameras in an automated factory setting for inspection or robotic vision. Its design objectives embody several ideas that are essential to practical, powerful systems:

First, it has 8-bit gray-scale image resolution. This is important, because lighting can vary considerably, making simple threshold comparisons (for example, in finding edges) misleading. Gray scale can also diminish errors caused by shadows or reflected glare and permit considerably greater definition of subject features for—in particular—identifying defects.

In addition, substantial processing power must be available, in order to obtain useful results essentially in real time. It must have robust algorithms that can take advantage of the gray-scale resolution to yield accurate, reliable results for a wide range of applications in real-world settings. It must be easy both for programmers (e.g., quality assurance engineers) to program and factory personnel to use. Finally, it must be cost effective.

These objectives have been met in the IVS-100, which uses model-based image processing (i.e., comparing the actual image with a stored model of the expected image) to reduce the computational overhead in acquiring the image and locating features. The basic system includes floppy and Winchester disk drives, camera, terminal, and monitor. Physically, it is housed in an 8 3/4"H × 19"-rack-mountable enclosure. It will be available in the U.S. in the Fall of 1984, priced under $30,000.

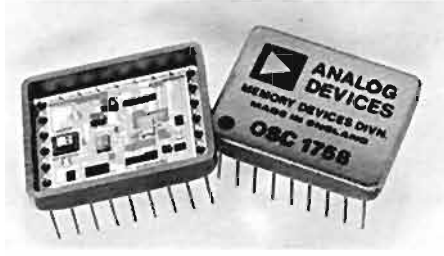
POWER OSCILLATOR FOR RESOLVERS

OSC1758 Provides 215 mA at 7V RMS at up to 10kHz
Use Its Sine-Wave Output for Resolvers, Inductosyns, LVDTs

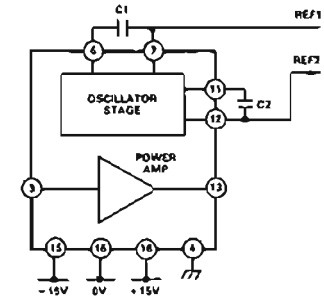
The OSC1758* is a power oscillator in an 18-pin double-width hybrid DIP. It provides a sinewave output of up to 215 milliamperes at 7 volts rms, at frequencies from 0 to 10 kHz. Although designed primarily to provide excitation for resolvers and Inductosyns†, it can also be used for LVDTs and RVDTs, as well as other devices, for up to 1.5 W.

As the block diagram shows, the OSC1758 comprises two independent parts, an oscillator and a power amplifier. The oscillator has two outputs phased at 90° to one another (2.5 V ±5% at 3 mA rms); the power amplifier has a gain of 2.8 (±1%) and is externally short-circuit protected. For power output at voltages less than 7 V rms, an external resistor is used to attenuate the input to the power amplifier.

*For technical data use the reply card.
†Inductosyn is a registered trademark of Farrand Controls, Inc.



The oscillator frequency is programmable by two identical external capacitors. Nominal frequency stability is ± 5%. Two temperature-range options are available, priced at $81 and $89 in 100s.



Worth Reading

NEW PUBLICATIONS FROM ANALOG DEVICES

Unless noted otherwise, all publications listed here are available free upon request; use the reply card.

Angular and Linear Data Conversion

Free 12-page brochure summarizes the Analog Devices line of synchro-, resolver, and Inductosyn†-to-digital converters with resolutions from 10 to 16 bits. Products range from a 3-chip hybrid to a 3-channel Multibus†-compatible board for multi-axis control.

Applications Guide for Isolation Amplifiers

Free 16-page brochure – written to help the designer understand where and how to apply isolation amplifiers to solve many of the common measurement problems encountered in industrial, instrumentation, and medical applications - describes 16 common applications of isolation amplifiers; it also describes their general characteristics and defines key specifications.

Analog/Digital Input/Output for MACSYM Systems

Free 68-page booklet is the completely updated and revised 1984 edition of the "ADIO Catalog." It includes electrical and mechanical information on cards and accessories for measurement input, analog output, discrete input/output, pulse I/O and clock functions, and special functions for MACSYM systems.

MCDigest "The Measurement and Control Digest published by Analog Devices, Inc.," is a quarterly publication of applications information, user feedback, and general information on system products of ADI's Measurement and Control Division. Volume 3, Number 4 (March, 1984), features a 6-page article on continuous control strategies—plus a number of helpful briefs, descriptions of new accessories and enhancements for MACSYM and other system products, messages from Customer Service, and Classified Ads. For your copy, or to subscribe, write to Applications Engineering, Analog Devices Measurement and Control Systems, 3 Technology Way, Norwood MA 02062.

IN BRIEF...

"Understanding LOGDACS™" – a free 4-page application note explaining essential theory and application of LOGDACs – d/a converters which provide a binary-input-to-logarithmic-gain rather than a binary-to-linear output function. The Analog Devices AD7100 series of CMOS multiplying DACs are discussed, along with the application benefits that wide-dynamic-range DACs can provide.

"RTI Series Microcomputer-Compatible Analog I/O Boards" - Two-page guide provides a quick reference to and selection guide for analog I/O boards to mate with VMEbus, MULTIBUS, STD bus, Micromodule bus, TM990 bus, and LSI bus.

"3B Series. Universal Signal Conditioning Front End for Any System." – An 8-page color brochure describing the 3B concept and products: a low-cost and versatile method of interconnecting a wide variety of real-world analog signals to computer-based systems, programmable controllers, and other industrial measurement-and-control systems.

Recent Articles in the Trade Press by Analog Devices Authors

"Single-Port Multiplier Reduces DSP-System Costs" by Doug Garde. *EDN*, January, 1984. (ADSP1110)

†Inductosyn is a trademark of Farrand Controls, Inc.; Multibus is a trademark of Intel Corporation.

"8-Bit A/D Converter Mates Transducers with μPs" by Mercer and Doug Grant. *Electronic Design*. January 12, 1984. (AD670)

"Instrumentation Amplifiers Solve Unusual Design Problems" by Scott Wurcer and Walt Jung. *EDN*. August 4, 1983. (AD524 & AD624)

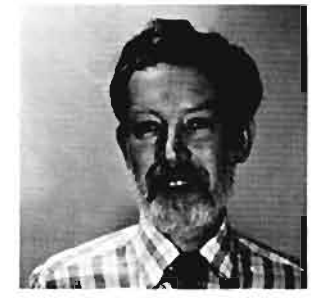
"RMS-DC Converter Chip Broadens Its Range" by Lew Counts & John Sylvan. *Electronic Design*. September 1, 1983. (AD637)

MORE AUTHORS *(continued from page 2)*

Steve Lewis (page 7) is a Group Leader in the Converter Design Department at Analog Devices Semiconductor. He joined ADS in 1979 after a varied early career including: a BA in Communications/ Political Science from Antioch, extracting Giant Neurons from squids at Woods Hole, Mass., engineering community-owned FM radio stations; and a BSEE from the University of Cincinnati. Since joining ADS, he has been involved in ADC and DAC design.

Jerry Neal (page 10) is a Regional Marketing Engineer at ADI's Computer Labs Division, in Greensboro, NC. See a more-complete biographical sketch and photo in *Dialogue* 17-1, page 2.

John Oxaal (page 3) is a Product Marketing Manager on the staff of ADI's Digital Signal-Processing Division. A more-complete biographical sketch and photo appear in *Dialogue* 17-1, page 26.



Per Pedersen (page 8) is a Design Engineer at Dantec Elektronik, in Denmark, working on the development of digital signal-analysis equipment. Graduated from the Technical University of Denmark (MScEE), he has worked with Regnecentralen for 12 years, developing two generations of computers. Later, as Systems Engineer at the European Space Agency in Germany, he designed ground-station data links for the METEOSAT and the OTS satellite.

Jim Surber (page 10) is an Applications Engineer at ADI's Computer Labs Division. After joining Computer Labs in 1975, Jim supervised the modular and card-level product-test facilities; he moved to his present position in 1983. Jim is also a full-time evening student at Guilford College, where he is pursuing a BAS degree in Management.

Bill Windsor (page 8) is a Product Marketing Specialist at ADI's Digital Signal Processing Division. A more-complete biographical sketch and photograph appear in *Analog Dialogue* 17-2, page 26.

Scott Wurcer (page 19) is a Design Engineer at Analog Devices Semiconductor. A more-complete biographical sketch and photograph appear in *Analog Dialogue* 17-2, page 26.

Potpourri

An Eclectic Collection of Miscellaneous Items of Timely and Topical Interest. Further Information on Products Mentioned Here May Be Obtained Via the Reply Card.

IN THE LAST ISSUE . . . (Volume 18, Number 1, 1984 — 32 pages):

Amplifier Noise Revisited - and a New Fixture for Automatic Noise Testing
Second-Generation Monolithic RMS-to-DC Converter (AD637)
Approximating Functions with Digital Signal-Processing ICs
75-MHz Conversions with 6-Bit Monolithic Flash ADC (AD9000)
Rate-of-Cooling Meter for Cryogenic Applications (featuring AD595)
Monolithic CMOS Triple-Output DC-DC Converter (AD7560)
Complete Monolithic 8-Bit, 10-microsecond A/D Converter (AD670)
New-Product Briefs:
- Low-Noise Op Amp: 0.18 microvolts p-p max (AD OP-27)
- Monolithic Temperature Sensors in Plastic Package (AD592)
- Monolithic 12-Bit DAC Family (AD DAC80, DAC85, DAC87)
- Highest-Resolution, -Speed Track-Holds
  - First Hybrid 14-Bit Track-Hold (AD389)
  - Fastest Acquisition Time: 14 ns typical, 19 max to 0.1% (HTS-0010)
- 12 X 12 CMOS Multipliers and Multiplier-Accumulators (ADSP-1012, -1009)
- Test Boards for Fast MCT-Handler-Based Tests of Digital ICs
- 12-Bit Hybrid Inductosyn/Resolver-Digital Converter (IRDC1732)
- uP-Controlled 12-Bit 3-Axis Resolver/Inductosyn Conversion (MCI-1794)

New Analog Devices Division Fellow Named: Lew Counts
Worth Reading: Noise Bibliography, RMS Application Guide, Short-Form Catalogs on High-Speed Conversion Products and Component Testers
Editor's Notes, Authors, Potpourri, Advertisement

INFRASTRUCTURE AS WELL AS INNOVATION . . . ESD - Electrostatic Discharge poses real headaches, especially for manufacturers and users of integrated circuits. We've prepared a 40-page booklet - ESD Prevention Manual - by Robert C. Kerns and Jeffrey R. Riskin, to help you understand and deal with the ESD problem. It's free; just ask for it on the reply card . . . What's the story on Leadless Chip Carriers (LCCs)? If you look at the front cover, you will understand why designers are attracted to LCCs: That little feller, with its 28 contacts for surface mounting, has the exact same AD667 chip as the bigger hermetic ceramic and plastic DIP packages pictured alongside. More and more Analog Devices IC products are becoming available in LCCs, including the AD574A 12-bit ADC and most of our op amps, ADCs and DACs. For information, get in touch with your nearby ADI sales engineer . . . Did you ever wish for the benefits of military-type processing (e.g., visual inspection, stabilization bake, temperature cycle or equivalent, constant acceleration, hermeticity, burn-in) with the stock availability and the lower temperature range and price levels of commercial-grade components (at minimal extra cost)? Now such parts, both bipolar and CMOS, hermetic and plastic, are available from Analog Devices in our PLUS program. Ask your nearby sales engineer . . . Wallchart available: An attractive 22" X 30" wall chart, entitled "Op-Amp User's Guide," has 15 application circuits, 3 tables, and amplifier selection information. Free while they last; ask your sales engineer . . . For best results - if you use a strong water spray and air dry for boards on which modules are mounted, pre-mount only fully potted (encapsulated) modules; mount "dummy-potted" modules after the water-wash cycle. If you're at all in doubt about units you're using, consult our applications or sales engineers.

THERMOCOUPLE CONDITIONING DEMONSTRATOR . . . If you've been considering the use of the AD594 and AD595 monolithic cold-junction-compensated thermocouple amplifiers, but wanted to see a working demonstration before deciding to design them in, we have good news for you. Our field-sales personnel now have portable demo setups, which function in both thermocouple and stand-alone temperature-monitoring modes, with digital readout in degrees Celsius. For action, call your local sales engineer.

NEW DATA SHEETS, ERRATA, ETC. . . . There is a new, updated data sheet available for the AD2050/51 uP-based thermocouple meters (C691b-15-4/84). If you're inquiring about the new AD2060/61 autoranging RTD meters (page 21), why not order a new AD2050/51 data sheet at the same time? . . . The HTS-0025 hybrid track/hold once shared a data sheet with the HTC-0300 series; but now it has its own expanded data sheet (C818-9-2/84) - and the HTC-0300 series (C698-9-482) has had its own for some time. Order these data sheets to replace the old combined one, which they supersede . . . Analog Dialogue 18-1 erratum: page 25, figure 4 - On the APPLE peripheral connector, the correct number of the Device Select pin is 41 (48 is already used for D1) . . . Corrections to AD293/294 data sheets in the 1982 DATABOOK: pages 5-28 (Vol. I) and 5-8 (Vol. II), pin 36 is -13V and pin 37 is NC (they were interchanged). This will have been fixed in the 1984 DATABOOK.

PATENTS AND AWARDS . . . 4,427,973 to A. Paul Brokaw and Modesto A. Maidique for "A-to-D Converter of the Successive-Approximation Type," i.e., the AD571 . . . 4,439,724 to William H. Morong, III, for "Apparatus for Determining the Number of Turns of a Magnetic Coil." . . . Barrie Gilbert, Division Fellow at Analog Devices Semiconductor, has been elected a Fellow of the IEEE . . . Three technical publications of ADI's Measurement and Control Division have been granted the "1984 Award of Excellence" in the annual publications competition of the Boston Chapter of the Society for Technical Communication. Tops in their respective classes were MCDigest (Periodicals - see facing page), the MACSYM 350 Documentation Set* (Document Sets), and the uMAC-5000 Command Reference Manual* (Consumer Manuals). The MACSYM 350 Documentation Set went on to win the international competition.
*Not a free publication. For information, write to MCS Marketing, Analog Devices, 3 Technology Way, Norwood MA 02062.

PRODUCT NOTES . . . Systems Notes (for information, consult Systems Sales): MACSYM 150 (new and/or upgraded) is now available configured for 512KB of memory. Higher compliance voltage (to 30V) is available in serial interfacing with MACSYM, using the DSI101 Serial Interface card. The AOC07 12-bit Analog Output Card for MACSYM is isolated, can retain data when used with an external supply, won't go to zero on Reset or change output on powerup, and allows the output value it is holding to be read back into the system . . . uMAC-5000 is now being shipped with REV 1.1 software . . . On AD7550BD, the new spec for VINH for the "Start" input, pin 14, is 3.0 volts max . . . The SDC1740 family now have substantially less dissipation, 0.86 W max (formerly 1.8 W max), and reduced chip count (down to 6 chips from 15) due to the introduction of an LSI chip . . . Please note that chassis-mount ac/dc power supplies in CM-2 cases have threaded inserts for #4 bolts . . . If you have difficulty with latchup in ADC1143 or out-of-range trims on DAC1146, get in touch with our customer-service representatives immediately for replacements; the problems have been identified and corrected on these types . . . In certain DSP products (16 X 16 and 12 X 12 multipliers and multiplier/accumulators), the I_{DD} quiescent specification with V_{IN} = 2.4 V has been revised to 25 mA (commercial temperature range) and 30 mA (military temperature range) from 15 mA and 20 mA, respectively.

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